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Dependence of VCO jitter on coupled noise

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Dependence of VCO Jitter on Coupled Noise

by

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Abstract

In mixed signal systems, the Phase Locked Loop (PLL) forms an integral part of the clock distribution scheme. The PLL is used to generate a local clock frequency, which is much higher than the external clock. The performance of a PLL is greatly influenced by the Voltage Controlled Oscillator (VCO). Any non-linearity introduced by the VCO affects the synchronization between operation of on-chip circuitry and the external components. The jitter or phase noise of a VCO is the most important non-ideality. Phase noise or jitter becomes critical as system frequency increases. The source of timing error maybe due to various noise sources, with power supply noise and that due to substrate coupling being the major contributors. The thesis presented here deals with the effect of these two noise sources on the time period of the VCO. The peak cycle jitter and cycle-to-cycle jitter due to noise is estimated by developing a relation between the noise source and the deviation in the output voltage in terms of the circuit parameters. First crossing theory approximation has been used to convert the voltage error to timing error. The theory has been extended to analyze the timing error when the two noise sources are present together. Good agreement has been shown between the theoretical prediction and the simulated result. The analysis can be extended to any number of stages for any operating frequency as will be demonstrated in the subsequent chapters.

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Chapter 1

Introduction

1.1 Background and Application

Most digital and mixed signal systems have a Phase Locked Loop (PLL) as an integral part of the clock distribution scheme. In simple terms, the function of PLL is to compare the output phase with the input phase and generate a corresponding phase error and accordingly generate a local oscillator frequency. The following block diagram illustrates the components that constitute the PLL.

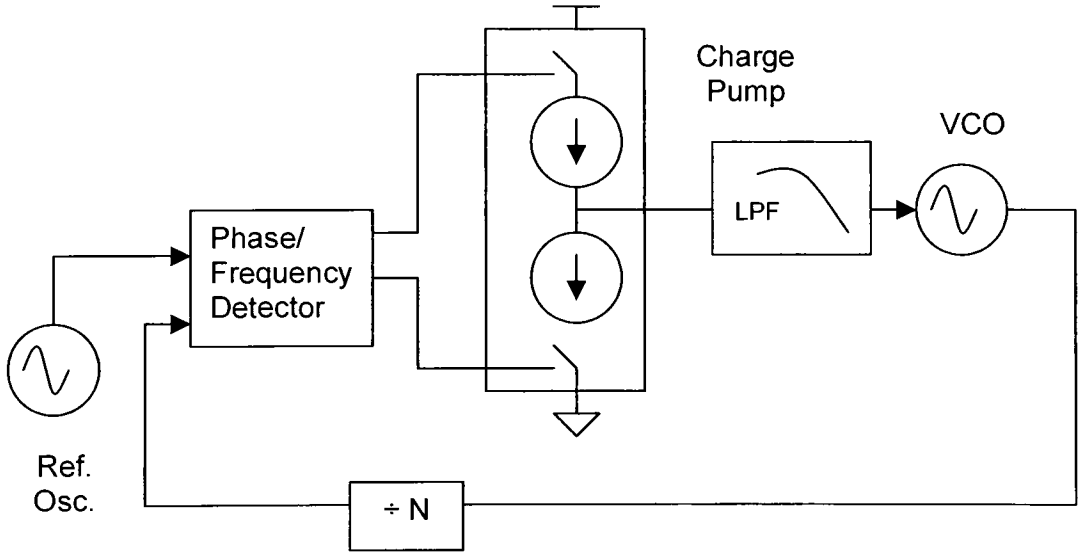


Fig 1.1 Basic PLL Schematic

The PLL consists of a reference oscillator, which generates the external clock frequency, phase/frequency detector, charge pump, loop filter, voltage controlled oscillator (VCO) and divider. With a constant divisor of N, the loop forces the VCO frequency to be exactly N times the reference frequency. The phase/frequency detector is normally constructed using D-FF's and AND gate. The charge pump which is shown as current sources are basically CMOS transistors. The charge pump along with the phase/frequency detector produces either positive or negative charge pulses depending on whether the reference signal phase leads or lags the divided VCO signal phase. These charge pulses are integrated by the loop filter (low pass filter) to generate a DC control voltage, which would then alter the VCO frequency until the phases are synchronized. The output frequency of the VCO is generally given by the following equation

$$f_{out} = f_c + K_{VCO}.V_{CTRL}$$

where, f_c is the free running frequency of the VCO under normal biasing conditions. The term K_{VCO} represents the sensitivity of the VCO to the DC control voltage. The term free running frequency means that the VCO is not receiving any correction pulses from the PLL.

The purpose of using a VCO is to synchronize the operation of on-chip components with the external oscillator. The timing accuracy of the clock signal

determines the maximum clock rate and hence the maximum number of operations per unit time[1]. The clock rate is determined by the sum of the setup time and hold time and it should have allowance for any timing jitter. In the case of wireless applications, the PLL is used to generate the local oscillator input to the mixer. The spectral purity of the Local Oscillators (LO) in both the receiver and transmitter is one of the factors limiting the channel-to-channel spacing and thereby reduces the maximum number of channels available. Similarly, in RADAR systems, the reduction of phase noise improves the receiver's sensitivity to low-level signals[2]. Other applications for PLL's and VCO's can be found in clock and data recovery systems and in disk-drive read channels. In these systems, they are used to generate a synchronized sampling signal. VCO's are also used to construct frequency synthesizers, which are used to generate clock frequency that is much higher than the external clock frequency. Such design also finds its use in RF transceiver applications.

Being an integral part of many high frequency operations, we need to look at some of the commonly found non-idealities in PLL circuits.

1. Dead zone: This non-ideality arises when the input phase difference $\Delta\Phi$ falls below a certain level Φ_0. When this happens the phase detector will not produce an output that would have reached any logic level. As a result, the charge pump will not send any correction pulse(s) and the VCO continues to accumulate the timing error.

2. Mismatch in charge pump: The mismatch is caused due to the difference in the drain currents of the PMOS and NMOS transistors. The reason is, it is very difficult to size the transistors such that the conductances of the transistors are same. As a result, the net current is never zero and a control voltage is constantly supplied to the VCO.

3. Jitter: This is the most important non-ideality in a PLL. The frequency domain representation is called 'Phase Noise'. Jitter is defined as the deviation of a signal from its ideal position in time. The noise sources which cause this timing error can be classified into two categories namely the interference noise and the device noise. The interference noise includes the noise on the power supply, the substrate (ground) noise and cross-talk[3]. The device noise includes the thermal noise, shot noise and the flicker noise (1/f noise). Out of these different sources, the noise from Power Distribution System (PDS) and that due to substrate coupling are the major contributors[4]. The thermal noise, even though it is the fundamental noise source in any circuit, is not analyzed here. There has been sufficient work that has been done in determining phase noise due to thermal noise effects and the expressions are given as part of the chapter containing previous work in this field.

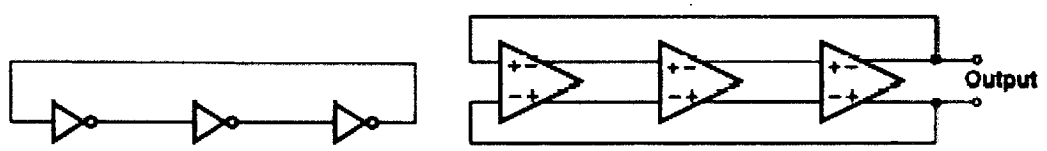
Phase noise or Jitter in the PLL becomes critical as the system frequency increases. With clock frequency in the hundreds of megahertz, clock skew

assumes added importance. Since the phase noise or jitter of the VCO dominates the performance of the PLL, reducing jitter in the VCO becomes even more critical. Even in traditional VCO circuits, such as the current starved ring oscillator, accurate analysis of jitter is a critical step in the design[4].

1.2 VCO Configurations

The oscillators can be broadly classified into Ring Oscillators and Harmonic Oscillators [3]. The most commonly used on-chip oscillators are the current starved ring oscillators. This is because of their ease of integration and also large tuning range. The harmonic oscillator uses passive components like inductors and resistors. The commonly used harmonic oscillators are LC tuned Oscillator and Relaxation Oscillator. The disadvantage of these configurations is that they occupy a lot of chip area and also the inductor values will be very high for lower frequencies and therefore they are more suitable for RF operations. On the other hand, the current starved ring oscillator uses standard CMOS technology without inductors or resistors. But the advantage of using harmonic oscillator is that, they require fewer stages (typically one stage) and therefore the number of noise sources is smaller than what is present in conventional ring oscillators.

The commonly used configurations for the oscillator, irrespective of whether it is a ring oscillator or a harmonic oscillator, are the single ended and differential ended ring oscillator. The block diagram for both is as shown here.



(a) (b)

Fig. 1.2 (a) Single Ended Oscillator and (b) Differential Oscillator

The differential oscillators can be constructed with an even number of stages (this can be done by connecting the inverted output to the inverting input of the next stage instead of connecting to the non-inverting input), whereas the single ended oscillators need an odd number of stages for oscillation to occur. The differential oscillator has the inherent advantage of better noise rejection and is less affected by supply and substrate noise when compared with the single ended oscillators. However, they are still impacted by these noise sources because of the following factors[5],

1. The diffusion capacitances at the delay stage output are modulated by the supply and substrate noise.
2. The threshold voltages of the input transistors are still affected by the substrate noise because of body effect.

3. Charge injection through the parasitic capacitance into the common source stage of the differential inverter results in phase noise.

Also, the differential oscillator has one extra noise source, which is due to the presence of the tail current transistor. According to [1] the low frequency noise or 1/f noise of this tail current source plays an important role in determining the phase noise or jitter of a VCO.

1.3 Thesis Outline

The thesis presented here consists of analysis done on jitter in VCO, caused by the noise on the PDS and noise due to substrate coupling effects. The objective of the analysis is to determine the contribution towards jitter by each of these sources. The initial analysis considers that the noise sources are present separately but later, the two noise sources are simulated when they are present simultaneously. This can be done because the noise sources considered in our analysis are uncorrelated. Even though the oscillator noise affects the amplitude also, it is not considered in our analysis. This is due to the fact that amplitude variations can be limited by using an Automatic Gain Control (AGC) mechanism [8]. Irrespective of the noise source considered, the theoretical analysis involves determining the transfer function between the noise and the deviation in the output voltage of the inverter. From ΔV we can obtain the timing deviation (ΔT)

using the first crossing theory [13]. The analysis involves the use of a single stage of the inverter and extending the results obtained to the entire VCO. Previous work [7] with supply and substrate noise effects on jitter has derived an expression for the RMS values for jitter but in the work presented here, effort has been made to determine the peak value of jitter. Depending on the specification for the VCO for its peak jitter, we can back calculate and see how the PDS can be designed or how the chip can be placed on the package so that the magnitude of noise can be reduced in order to be within the specification for the maximum allowable jitter. Similarly, measures can be taken to reduce the substrate coupling effects as well.

1.4 Organization

The second chapter introduces definitions for some terms like jitter, long-term jitter, cycle jitter and cycle-to-cycle jitter. The time domain terms are also linked to frequency domain parameters. The test circuit that has been considered for the analysis is also presented. Important points about designing a VCO are discussed here. The chapter also has a brief description about prior work that has been done in determining jitter or phase noise in a VCO.

Chapter 3 contains the first part of the theoretical analysis. It involves studying the effect of PDS noise on jitter. The chapter contains the simulation results obtained and explanation associated with them.

The substrate coupling effect is studied in Chapter 4. The chapter includes the details about the theory we have used to determine the relation between noise from the substrate and the jitter of a VCO. A comparison is drawn between the theory adopted and the simulation results obtained. As a sub-section, the results of simulating the PDS noise along with the substrate noise have also been shown here.

Finally, Chapter 5 summarizes the results obtained along with the conclusion. Future work that can be done on the work presented is also discussed here.

Chapter 2

Background

In this chapter, a brief description about jitter and the different ways to express jitter of a VCO is given. The second section has the frequency domain representation of jitter. Also, a link between the time domain and frequency domain representation is provided. The third section contains the test circuit that we have used for the theoretical analysis and the final section of the chapter lists some of the previous work that has been done in order to determine the relation between jitter of the VCO and noise on the PDS and noise due to substrate coupling effect.

2.1 Definition of Jitter

In time domain representation, normally the spacing between the zero crossings of the oscillator output is ideally constant. However, the spacing may be variable due to some noise fluctuations. This timing uncertainty is called "Jitter". Jitter can be defined as "deviation of signal from its ideal position in time" For a free running oscillator, any uncertainty in the previous transition affects all the following transitions, and the effect persists indefinitely. The reason for studying timing error is so important because, the time deviation affects the locking of the on-chip oscillator with the external oscillator, which may

in turn disturb the synchronization between different digital circuitry. There have been various terms to define jitter namely long-term jitter, cycle jitter and cycle-to-cycle jitter. They can be explained using the following figure [7].

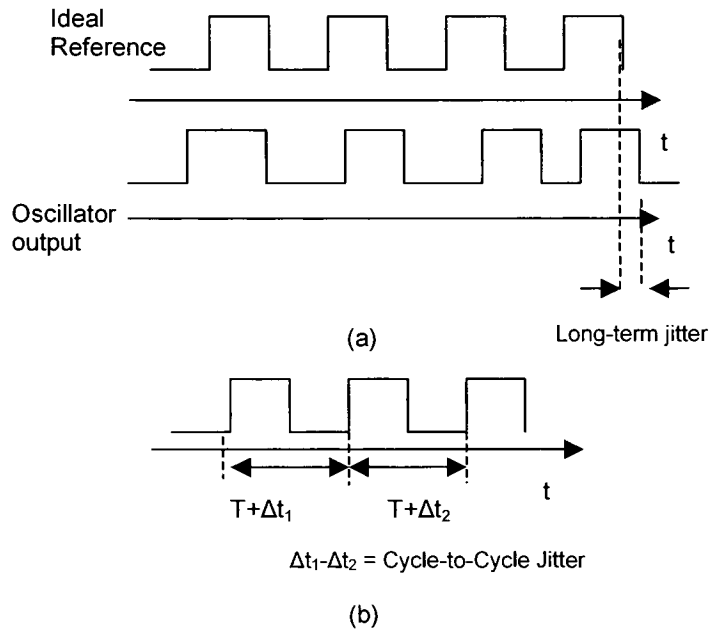


Fig. 2.1 (a) Long-term Jitter Representation (b) Cycle-to-Cycle Jitter Representation

Absolute jitter or long-term jitter is given by the following expression

$$\Delta T_{abs}(N) = \sum \Delta T_n$$

But, this quantity does not define the performance of the oscillator as the variance of ΔT_{abs} diverges with time. This is because, a free running oscillator tends to accumulate jitter. Also, depending upon the bandwidth of the PLL, it should be able to send correction pulses to try to reduce the long-term jitter.

Hence, the long-term jitter strongly depends on the PLL dynamics and it is not of much interest for design issues.

The second type of jitter is called the Cycle Jitter. The cycle jitter compares the present period with the mean period of the oscillator. The RMS value of cycle jitter is given by the following formula

$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2}$$

The cycle jitter gives an idea about the variation of the period with respect to its mean period and the parameter is useful when dealing with the effect of low frequency noise on jitter or phase noise.

The third type of jitter considered normally for describing the performance of a VCO is the cycle-to-cycle jitter. The expression for the same is given by

$$\Delta T_{cc} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} (T_{n+1} - T_n)^2}$$

The cycle-to-cycle jitter compares the period with its preceding period and hence it describes the short-term dynamics of the period. But here, the long-term dynamics are not characterized. If 1/f noise modulates the frequency slowly, then

ΔT_{cc} does not reflect the result accurately. This is because the value of ΔT_{cc} might not vary at all whereas the time period would have drifted away from the mean period. In these cases, the cycle jitter is a better measure of timing error. In the analysis presented here we consider cycle-to-cycle and cycle jitter but we do not derive the relationship in terms of RMS values, but we compute the peak jitter value instead.

2.2 Phase noise expression

In frequency domain, the noise spectral density characterizes the oscillator's timing error. The phase noise is the ratio of the sideband power at an offset frequency to the carrier power. The above can be explained by using the following expression [5],

$$L(\Delta\omega) = 10.\log[P_{sideband}(\omega_0 + \Delta\omega, 1Hz)/P_{carrier}]$$

where $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ represents the single sideband power at an offset frequency $\Delta\omega$ from the carrier frequency and the measurement bandwidth is 1Hz. $P_{carrier}$ is the total power under the power spectrum. But, the problem with the above expression is that it includes both amplitude and phase noise in it. But by using gain control techniques the effect of amplitude noise can be reduced. The important parameter is the phase part, which is called the phase noise. The

unit for phase noise is dBc/Hz. A value of -100dBc/Hz at an offset frequency means that the signal level at that frequency is 100dB below the carrier level. To properly define phase noise it is important to include the phase noise information and the corresponding offset frequency. The above expression is the basis for the derivation of phase noise due to different noise sources.

There has been literature [8], which gives a relation between the time domain representation and phase noise. The expression is provided here just to provide a link between time domain and frequency domain measurements,

$$\Delta T_c = \frac{f_m}{f_0}\sqrt{S_\phi(f_m)}\sqrt{T} \qquad \Delta T_{cc} = \frac{\sqrt{D_\phi}}{\Pi f_0^{3/2}}$$

where, ΔT_c and ΔT_{cc} are the rms values for cycle jitter and cycle-to-cycle jitter respectively, T is the average time period of the oscillator, f_o is the normal oscillator frequency, f_m represents the offset from f_o, $S_\Phi(f_m)$ represents the sideband phase noise and D_Φ is called the phase diffusivity and is given by the following relation

$$S_\phi = \frac{D_\phi}{2\Pi^2 f_m^2}$$

2.3 Circuit Description

The circuit of interest here is the current starved inverter. The two common configurations of the current starved inverter are the single ended and the differential ended ring oscillators. For the analysis presented here, a single ended oscillator has been used. The operating frequency of the oscillator is determined by the propagation delay of each stage of the inverter in the ring oscillator. Assuming symmetric rise time and fall time, the time period of the oscillator is given by the expression

$$T=2*N*t_d$$

where N is the number of stages of inverter and t_d is the propagation delay of a single stage. The control voltage Vc in figure 2.2 controls the current that flows in the bias network, which in turn controls the current that flows in the current starved inverter. Hence, we can control the propagation delay of the inverter and in turn the time period by varying the control voltage. The effective resistance and capacitance at the output of the inverter stage also affects the propagation delay. The output resistance is the combination of the PMOS load and the NMOS load, and the capacitance seen is the gate capacitance of the next stage added with the parasitic capacitance. The resistance values are pretty low, the reason being that the DC currents are high (in the order of a few hundred μA) and the

capacitance values are in the order of a few pF's. As a result, a single stage delay was found to be about 1.83ns. The other variable which affects the time period is the number of stages of the inverters. The minimum number of stages to cause oscillation is three.

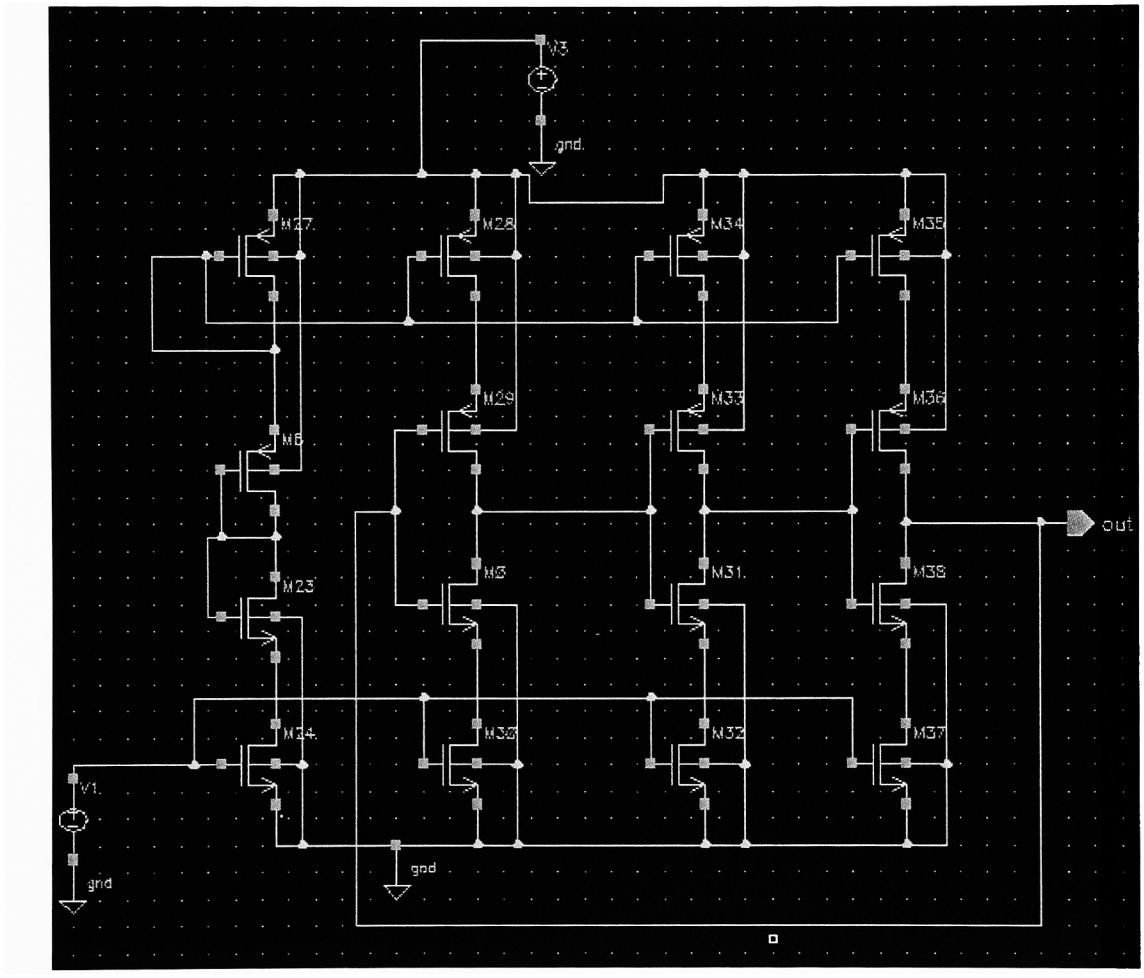


Fig. 2.2 3-Stage Current Starved Ring Oscillator

In the test case taken here for analysis, the operating frequency of the oscillator is set to be 180MHz (time period of 5.51ns). If the frequency of the VCO needs to be increased, then the current supplied should be more. But, this will cause an increase in power dissipation. But by supplying more current there is the advantage that the rise time is smaller, which means that the time during which the circuit is susceptible to jitter is shorter and hence the sensitivity of the VCO towards noise source is less. So, there is a trade-off between power dissipation and jitter of the VCO.

The following table contains the specifications of the test circuit used for the analysis.

Number of Stages (N)	3
Operating Frequency	180MHz
Bias Current	2uA
Power Dissipation	2.5mW

Table 2.1 Test Circuit Specifications

Important points to be considered for designing a VCO for low jitter

1. Increase the charging and discharging current.
2. Make the gate capacitance smaller. This can be done by reducing the widths of the input PMOS and NMOS transistors.

The above-mentioned are done in order to increase the slew rate and thereby to reduce the rise time of the VCO output.

3. Large signal swing implies higher SNR ratio. This is difficult to achieve because of low voltage power supplies that are available for design.
4. Addition of load capacitors to each stage helps to reduce jitter [7]. But, the capacitor should be placed inside a guard ring so as to reduce the substrate coupling effect.

2.4 Previous Work

Previously published papers and books have dealt in detail with the analysis of phase noise of a VCO. In the analysis presented here, time domain approach has been used. In [7], a simple inverter has been used instead of the current starved inverter considered in our analysis and an expression for rms jitter has been derived. In the analysis presented, they have considered power supply and substrate noise as the main sources for jitter. The paper further proves that the thermal noise is not an important noise source and that it contributes very less to the jitter of the VCO.

The expression for the rms values of cycle jitter and cycle-to-cycle jitter is as given below,

$$\Delta T_c = \frac{V_m K_0}{\sqrt{2} f_0^2} \qquad \Delta T_{cc} = \frac{V_m K_0 \omega_m}{\sqrt{2} f_0^3}$$

where ΔT_c and ΔT_{cc} are the rms values for cycle jitter and cycle-to-cycle jitter respectively, f_0 is the normal operating frequency of the oscillator, f_m is the frequency of noise on the power supply and K_0 is the static or low-frequency sensitivity of the VCO. The sensitivity is obtained from the slope of the curve connecting frequency and V_{DD}. The important conclusions that can be drawn from these equations are that, the rms value of cycle jitter is independent of the noise frequency whereas the cycle-to-cycle jitter value is dependent on the frequency of the noise signal and that it is to an extent linearly related to the jitter. The frequency dependency for cycle-to-cycle jitter can be understood from the fact that it compares the present period with the previous period. So, if the noise frequency is high, then the difference between consecutive time periods will be high as well. The paper has described substrate noise effects on rms jitter. According to the paper, the main source of jitter results from parasitic capacitances such as C_{db} and C_{sb}. The paper has also shown that the effect of supply and substrate noise on jitter is independent of the power dissipation. The

reason for this is, in the case of supply and substrate noise both the signal and noise voltage are increased by the same factor N (number of stages of inverter).

In [10], the analysis presented considers internal noise and the low frequency noise (1/f noise) as the main sources of phase noise. The paper has described an impulse sensitivity function which determines how sensitive the oscillator is to noise. The relation between phase noise, power drain of the oscillator and the number of stages has been derived in the paper.

The following are the expressions for phase noise for single ended and differential oscillators.

$$L\{\Delta f\} \approx \frac{8}{3\eta} * \frac{KT}{P} * \frac{V_{DD}}{V_{char}} * \frac{f_0^2}{\Delta f^2}$$

$$L_{min}\{\Delta f\} \approx \frac{8}{3\eta} * N * \frac{KT}{P} * \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}}\right) * \frac{f_0^2}{\Delta f^2}$$

where $L\{\Delta f\}$ is the phase noise, P is the power dissipation, N is the number of inverter stages, f_0 is the operating frequency of the oscillator, Δf is the offset frequency and V_{char} is ratio of gate-overdrive voltage to the short channel co-efficient.

Some of the important conclusions from their analysis are listed here,

1. For single ended ring oscillators, the phase noise is inversely proportional to the power dissipation.

2. The phase noise increases quadratically with operating frequency.
3. The phase noise of single ended oscillators does not depend on the number of stages of the inverters used.
4. The differential configuration has a strong dependence on the number of stages of inverters. The reason for this is, for N inverter stages, there are 2N noise sources in the differential configuration whereas, in the single ended configuration we still have only N noise sources.
5. The tail current transistor in differential configuration is the major contributor to phase noise.
6. The common mode sensitivity problem can be reduced to some extent by having two identical ring oscillators, which operate out of phase.

There have been other papers that have done theoretical analysis as to how to minimize jitter. In [5], a comparison has been done with different types of loads like single PMOS loads which are either in linear mode or in saturation mode and maneatis load. This is more a qualitative analysis than a quantitative analysis. The results obtained in the paper can be summarized as follows: Combined PMOS load performs better than single PMOS load but, the important conclusion arrived by them is that single ended oscillator can be as good as or even better than the differential oscillator in terms of phase noise.

In terms of work done to analyze substrate noise effects, the objective has been to model the generation and propagation of substrate noise [11] in the substrate. Also, the paper talks about how to minimize the effect of substrate noise at different levels namely the chip level, the system level and at the layout level. There have also been algorithms that have been developed which do the placement of chips based on the level of noise each circuit block can tolerate. But, the literatures have not clearly stated the relation between the substrate noise and how it is translated into timing jitter. Also, there has not been any work done to theoretically predict the jitter due to noise from the substrate coupling effect. In the analysis presented here, a theoretical solution has been shown, using which the maximum cycle jitter and cycle-to-cycle jitter of a VCO can be determined.

Chapter 3

Analysis of Effect of Power Supply Noise

This chapter contains the first part of the analysis which involves determining the jitter caused due to the noise on the power distribution system. A basic introduction as to how noise is induced on the power supply is provided in the first section. Some of the parasitics which act as noise sources are presented here. The second section introduces the method by which the noise voltage at the output of the inverter, due to the noise on the power supply is determined. A brief mention about first crossing theory which is used to obtain the timing error is also presented here. The simulation results obtained are provided in the third section. The simulation setup is briefly explained here. Both cycle jitter and cycle-to-cycle jitter due to different noise voltage amplitude and frequency combinations are shown. A comparison between the theoretical values obtained and that obtained from performing the simulations is presented in the fourth section. Explanations for the results obtained in which we found significant difference between the theoretical prediction and the simulated result are also provided as part of this section.

3.1 Noise on Power Supply

The noise on the power supply that affects the normal working of the chip is due to parasitics associated with the board and the parasitics associated with the packaging of the chip. In Printed Circuit Boards (PCB), the power and ground planes along with the vias form the power distribution system (PDS). A poorly designed PDS can result in non-idealities such as ground bounce, power supply compression and electromagnetic interference. The noise on the PDS can cause unintentional coupling between different parts on the board and this coupling noise can be significant enough to affect sensitive circuits like the VCO in our case. The parasitic inductance in the PDS offers finite impedance to the VCO circuit when they draw current from the power supply during switching. This results in generation of voltage fluctuation on the power supply and it is called as Delta-I noise [4]. The impedance can be characterized in terms of their self-impedance and trans-impedance. The magnitude of the delta-I noise depends on the current drawn by the VCO and the impedance at that node and is also affected by coupling noise caused due to the trans-impedance effect. The above-mentioned noise is due to the noise on the PDS, but the circuit can also be affected by noise added to the power supply from certain packaging issues at the chip level. After fabrication and dicing, integrated circuits need to be packaged. The parasitics associated with the package and the connections to the chip affect the performance of the circuit at high speeds and at high operating frequency [9].

Some of the commonly introduced parasitics while packaging are self-inductance of the bond wire, trace self-inductance, trace-to-ground capacitance, trace-to-trace mutual inductance, and trace-to-trace capacitance. As a result of this, the connections between the circuit on-chip and the external components are far from ideal. For theoretical purposes, we have assumed that there is already noise present in the power supply and the objective is to relate the jitter of the VCO to the noise on the power supply.

3.2 First Crossing theory

The first crossing theory is an approximation used to convert the noise voltage perturbation to timing error. The theory can be explained using the following figure. The two lines shown represent the output of the oscillator when it is not affected by noise and when it is affected by noise. The assumption made here is that the next stage of the inverter switches at exactly half of the voltage swing and that the error in the actual time of zero crossing, is the error that is passed onto the subsequent stages of the VCO [13, 14].

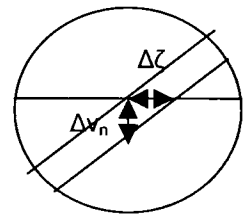


Fig. 3.1 First Crossing Theory Approximation

The relation between the timing error and noise voltage is given by

$$\Delta\tau^{-2} = \Delta v_n^2/(\text{Slew Rate})^2 \qquad (3.1)$$

where $\Delta\tau$ is the variation in the zero crossing time, Δv_n is the output noise voltage. From the first crossing theory equation we can observe that the timing error can be reduced by increasing the slew rate, which can be achieved by supplying more current or, by reducing the gate width of the input transistors. Making use of the approximation we can derive some important relations between the timing error and the voltage swing.

The time delay due to each stage of the inverter is given by

$$t_d = C_L V_{SW}/I_{SS} \qquad (3.2)$$

where t_d is the propagation delay, V_{SW} is the output voltage swing, C_L is the load capacitance at the output of each stage, and I_{SS} is the output current.

Normalizing the timing error to the time delay due to each stage we get

$$\frac{\overline{\Delta t_d^2}}{t_d^2} = \overline{\Delta v_n^2}.\left(\frac{C_L}{I_{SS}}\right)^2\left(\frac{I_{SS}}{C_L V_{SW}}\right)^2 \qquad (3.3)$$

which can be simplified into the following expression,

$$\frac{\Delta t_{d\,rms}}{t_d} = \frac{\Delta v_{n\,rms}}{V_{SW}} \qquad (3.4)$$

The important point to note here is that, increasing the voltage swing of the output can decrease the timing error.

3.2.1 Determination of the transfer function

Having determined the relation between the noise voltage and the timing error, it is now required to determine the transfer function between the noise on the PDS and the noise at the output of the inverter. The objective here is to find the relationship between the DC circuit parameters like the transconductance of the transistors, and the resistances and the noise at the output of the inverter. The analysis is based on the single stage of the current starved network (fig 3.2).

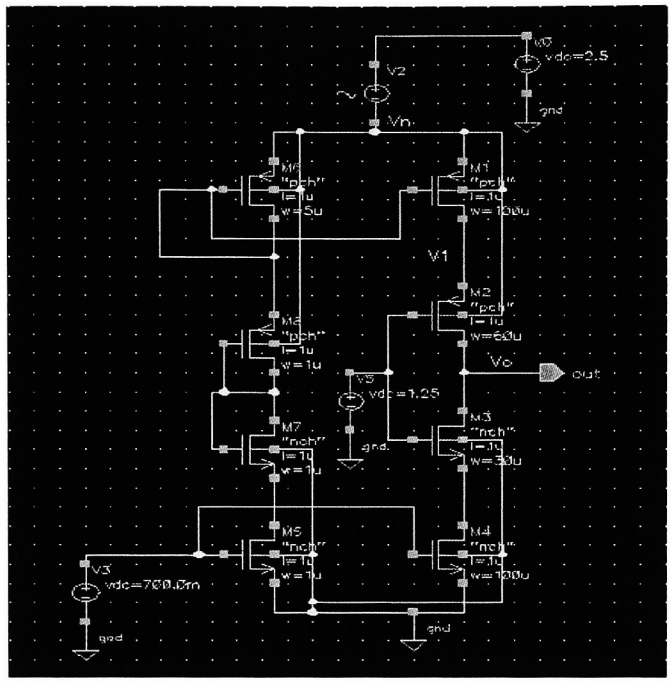


Fig 3.2 Single Stage of the Oscillator

To obtain the DC parameters, the input PMOS and NMOS transistors were connected to a DC voltage of 1.25 (which corresponds to the zero crossing voltage). As a result of doing this, we can consider the transistors to be current sources with a finite output resistance. The noise voltage on the power supply is assumed to be sinusoidal.

The AC small signal model of the circuit can be used for determining the transfer function. The small signal model is as shown below.

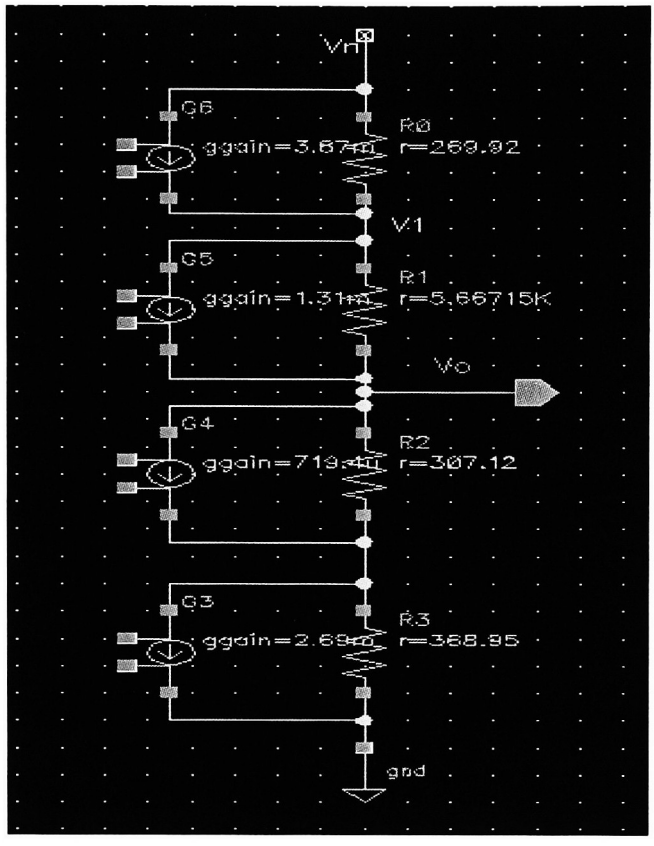


Fig 3.3 Small Signal Model

The underlying theory behind this analysis is that, the noise on the power supply is magnified by the gain provided by the current starved network.

The effective resistance at the output node of the inverter is given by the following expression,

$$R_0 = \{[1+ g_{m2}\, r_{02}]^* r_{01} + r_{02}\} \parallel \{[1+ g_{m3}\, r_{03}]^* r_{04} + r_{03}\} \qquad (3.5)$$

and the output voltage at the inverter can be approximated to

$$V_o/V_n = g_{m2} * R_0 \qquad (3.6)$$

In the above equations, V_n is the noise voltage amplitude on the power supply, V_0 is the noise voltage at the output of the inverter, g_{m1}, g_{m2}, g_{m3}, and g_{m4} are the transconductances of transistors M1, M2, M3 and M4 and r_{01}, r_{02}, r_{03}, and r_{04} are the output resistance of transistors M1, M2, M3 and M4 respectively.

The expression in equation (3.6) gives the gain provided by the first stage of the VCO. But, in order to determine the jitter of VCO we need to consider the three stages. If the noise variations were DC, then it would be enough if we multiply the deviation in output voltage obtained from the single stage analysis with the number of stages of the inverter. But here, the noise is assumed to be sinusoidal and as a result, there is a strong correlation between the three stages of the VCO. So, it is necessary to determine the transfer function between the noise on the power supply and output of each of the current starved network.

The transfer function between the output of the second and the third stages of the inverter are influenced by the noise at their respective input PMOS and NMOS transistors. The gain provided by the path from the power supply and the input transistors can be calculated separately and by using superposition

principle we can arrive at the desired transfer function between the noise on the power supply and the corresponding output voltage.

Consider the second stage for the calculation of the transfer function. The transfer function between the power supply and the output is the same as for the first stage. The transfer function between the input noise and the output can be calculated as follows. The magnitude of the gain provided by the input PMOS and NMOS transistors are

$$V_{0p}/V_{in} = g_{mp}*R_0 \text{ and } V_{0n}/V_{in} = g_{mn}*R_0 \qquad (3.7)$$

$$V_{02} = (V_{0p}+ V_{0n})*V_{in} \qquad (3.8)$$

where V_{02} is the contribution of output noise voltage due to input noise, V_{0p} and V_{0n} are the output noise voltage due to the PMOS and NMOS transistors respectively, g_{mp} and g_{mn} are their transconductance value, R_0 is the effective output resistance at the output of the inverter, and V_{in} represents the magnitude of noise voltage at the input of the transistor. For the second stage V_{in} represents the gain provided by the first stage, which is the transfer function derived before.

The objective is to obtain the transfer function between the power supply noise and the output voltage deviation. The gain provided by the input transistors are opposite in phase with respect to the gain offered by the current starved

network to the power supply. The effective transfer function will be the difference between the individual values.

$$TF_2 = \Delta V_0/\Delta V_{DD} = V_{02} - TF_{ps} \qquad (3.9)$$

where TF_2 is the transfer function of the second stage and TF_{ps} is the transfer function between the power supply and the output of the second stage.

Similarly, we can derive the transfer function for the third stage as well. The final equation relating the noise on the power supply to the output voltage deviation is as follows.

$$\Delta V = (TF_1 + TF_3)^* \Delta V_{DD} - TF_2^* \Delta V_{DD} \qquad (3.10)$$

where TF_1, TF_2 and TF_3 are the transfer functions between the first, second and third stage and the power supply and ΔV_{DD} is the power supply variation.

After obtaining the output noise voltage we can compute the resulting timing error using the first crossing theory. The objective of the analysis, as mentioned before, is to determine the maximum cycle jitter and cycle-to-cycle jitter. For this, we need to have a proper definition for the excess voltage at the

output of the inverter. The reason for this is, we are dealing with sinusoidal perturbation and therefore the time period varies as the noise voltage varies.

To determine the cycle jitter, a comparison is made between the time period of the VCO and its mean period. The maximum value of the cycle jitter occurs when the noise signal has reached its amplitude value. The excess voltage at the output of the inverter then is linearly related to the level of the noise signal above the DC power supply (=2.5v). Therefore, the cycle jitter will be linearly related to the noise amplitude and also, the cycle jitter will be the same irrespective of the frequency of the noise signal. This confirms the reason for the rms values of cycle jitter being independent of the noise frequency.

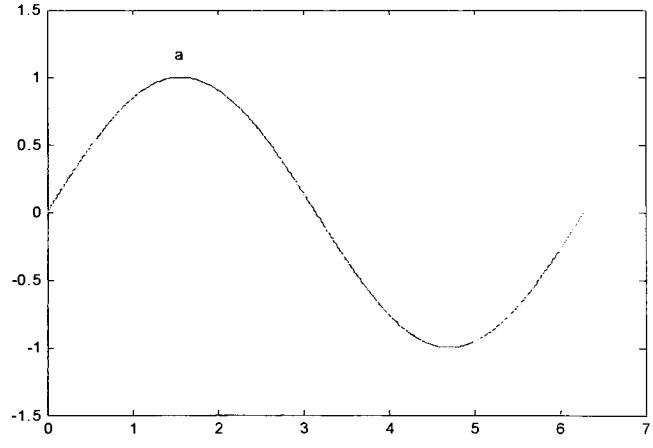


Fig 3.4 Noise Voltage on the Power Supply

But this will be true up to a noise frequency of 45MHz (1/4th of operating frequency). This can be explained with the help of the illustration shown in fig.

3.4. The point 'a' in the figure represents the peak value of the noise signal. For frequency value of say about 10 or 20MHz, the maximum value of cycle jitter theoretically will be the same, but when the noise frequency is greater than 45MHz, then the noise voltage seen by the VCO would be less than the amplitude value because the signal would have crossed the point 'a'. As a result of this, for frequencies greater than 45MHz, the VCO cycle jitter values will be smaller.

In the case of cycle-to-cycle jitter, we compare the present period with the preceding period. The maximum value of cycle-to-cycle jitter occurs when the noise voltage variation is the maximum between two consecutive time periods. This occurs when the noise voltage slope is the maximum. Looking at fig. 3.4 we can say that the peak value for cycle-to-cycle jitter would occur when the noise signal is changing from negative maximum to positive maximum or vice versa. Therefore the maximum change of voltage on the power supply will be a percentage of the peak-to-peak value of the noise signal. The percentage is determined by the frequency of the noise signal. As a result, what we find is that the maximum value of cycle-to-cycle jitter depends on both the frequency and the amplitude of the noise signal. The maximum value increases almost linearly as we increase the frequency up to ½ of the VCO frequency. For frequency values greater than ½ the VCO frequency, the maximum cycle-to-cycle jitter value will decrease. This is because the noise signal would have changed from its positive

peak to the negative peak before the VCO would have completed one period and hence, the maximum noise voltage variation will be smaller.

3.2.2 Calculations

This section presents the calculations performed to determine the maximum cycle jitter and cycle-to-cycle jitter. First, it is required to find the relation between the noise voltage and the deviation at the output of the inverter. By using the equations given in section 3.2 we can achieve this.

The following are the formulas used to determine the drain current, the transconductance of the transistors and the output resistance values [12].

$$I_{ds} = \frac{1}{2}\mu_{eff}C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \qquad (3.11)$$

$$g_m = \sqrt{2 * \mu C_{ox} * I_d * W/L} \qquad (3.12)$$

$$V_{ACLM} = \frac{A_{bulk}E_{satL} + V_{gst}}{A_{bulk}E_{satl}}(V_{ds} - V_{dsat}) \qquad (3.13)$$

$$r_0 = V_{ACLM}/I_d \qquad (3.14)$$

where V_{ACLM} is the Early voltage due to the channel length modulation effect and A_{bulk} is the term used to accommodate the bulk charge effect. This parameter is introduced because the threshold voltage varies along the length of the channel

owing to the non-uniform thickness of the channel formed along the channel length.

The expression for A_{bulk} is given by

$$A_{bulk} = (1 + \frac{K_1}{2\sqrt{\varphi_s - V_{bseff}}}\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}[1 - A_{gs}V_{gsteff}(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}})^2] + \frac{B_0}{W_{eff} + B_1}\})\frac{1}{1 + K_{ETA}V_{bseff}}$$

The explanation for the symbols in the above equation is given as part of the parameter definition in Appendix 2.

The drain current is determined by the control voltage of the VCO and it is fixed by design. In this design, the control voltage was chosen to be 0.7V and the drain current was found to be around 380μA. The transconductance values for transistors M1, M2, and M3 are 0.003868S 0.00132S and 0.0007355S respectively. The output resistance associated with the transistors M1, M2, M3 and M4 are 269.78 Ω, 5648.2 Ω, 311.244 Ω, and 374.7 Ω respectively. The gain offered by the first stage is then given by equation (2) and it is equal to

$$V_o/V_n = \{[1+(1.32e\text{-}3*5648.2)]*269.78+5648.2\} \| \{[1+(7.35e\text{-}4*311.2)]*374.7+311.2\}$$

which can be simplified into

$$V_o/V_n = \mathbf{0.9254}$$

This is the transfer function between the power supply and the output of the inverter irrespective of which stage of inverter it is.

Second stage: The transfer function between the input and output of the inverter is given by

$$V_{02} = g_{mp}*R_0 + g_{mn}*R_0 = (0.000131+0.0007194)*701.118 = \mathbf{1.44114}$$

$$TF_2 = V_{in}* V_{02} - TF_{ps} = (1.44114*0.9254)-0.9254 = \mathbf{0.40826}$$

Third stage: Here, the gain provided by the inverter to the noise on the power supply and the gain provided by the input transistors are in phase. The transfer function between the input and output of the inverter is the same as that for the second stage and is given by

$$V_{03} = \mathbf{1.44114}$$

The final transfer function between the power supply variation and the output of the inverter is then given by the sum of the individual transfer functions.

$$TF_3 = V_{in}* V_{03} + TF_{ps} = 0.92547*0.44114*1.44114+0.92547 = \mathbf{1.5138}$$

Therefore the final relation between the noise fluctuation on the power supply and the deviation in the output voltage in terms of the contribution of the individual stages is given by,

$$\Delta V = (TF_1+TF_3) * \Delta V_{DD} - TF_2 * \Delta V_{DD} = \mathbf{2.4392\ \Delta V_{DD} - 0.40826\ \Delta V_{DD}}$$

3.3 Simulation results

The simulations were performed using Affirma Analog Artist Design Environment. The BSIM model of a 0.25um process was used for both simulation and calculation purposes. From simulations the transfer function between the output of the inverter and the power supply was found to be 0.95, which matches well with the theoretical calculations.

To obtain the maximum cycle-to-cycle jitter, the difference in time period between consecutive outputs of the VCO was measured. A series of observations was taken for each of the noise signal to make sure that the peak value was covered in the simulation. The rms value of the cycle-to-cycle jitter was also calculated in order to show the disadvantage of characterizing the VCO jitter in terms of its rms value alone.

The simulations were done for noise voltage amplitude ranging from 10mv to 70mv with frequencies from 10MHz to 70MHz. The table shows the maximum cycle-to-cycle jitter values obtained from the simulations for the designed VCO.

Noise (mV) / Freq (MHz)	10	20	30	40	62.5	70
10	0.005380	0.017840	0.018680	0.019780	0.021680	0.025150
20	0.009880	0.020320	0.024260	0.028560	0.042570	0.048250
30	0.020640	0.023030	0.032560	0.039600	0.073660	0.065440
40	0.009560	0.020220	0.036500	0.048150	0.075310	0.081550
50	0.012930	0.030920	0.037610	0.047890	0.076240	0.087150
60	0.011460	0.030810	0.039190	0.050470	0.069130	0.090080
70	0.011250	0.022710	0.041280	0.049900	0.077190	0.077790

Table 3.1 Maximum Cycle-to-Cycle Jitter (ns)

The second type of jitter parameter of interest is the cycle jitter. In order to obtain this value from simulation, the difference between the present period and the mean period was calculated. Similar data sets for the noise amplitude and frequency were used to determine the jitter value and they are as shown in the

following table. The values shown in both the tables are the magnitude difference (in ns) between the time periods of interest.

Noise (mV) / Freq (MHz)	10	20	30	40	62.5	70
10	0.01595	0.10877	0.1199	0.1269	0.10554	0.1018
20	0.02398	0.10189	0.11215	0.12719	0.08324	0.11254
30	0.0956	0.09624	0.11359	0.12195	0.14003	0.10379
40	0.02249	0.01428	0.11143	0.11722	0.0825	0.08569
50	0.01555	0.09784	0.10653	0.11356	0.09483	0.13758
60	0.02898	0.09685	0.10623	0.11022	0.12415	0.13306
70	0.00919	0.01654	0.09936	0.11096	0.1228	0.13006

Table 3.2 Maximum Cycle Jitter (ns)

In the preceding section, we mentioned that the cycle jitter is independent of the noise signal frequency. But, if we look at the data values we see that it is not constant. The reason for this discrepancy is that the cycle jitter is due to the effect of a single noise voltage value. The assumption made in the theory is that the power supply voltage starts at 2.5V and starts varying according to the

amplitude and the frequency of the noise signal. Therefore, the mean period of the VCO should be approximately equal to the mean period of the VCO. But, when the simulations are performed it may so happen that the VCO sees a different magnitude of noise on the power supply. As a result, the timing error caused by this noise fluctuation will be different. This affects the next period and the effect persists indefinitely and the mean period of the observations taken will be less than the expected mean period, which should be around 5.5ns for our example VCO.

As a sub-result, the rms value of the cycle-to-cycle jitter is provided here and the theoretical calculations were done using the derivation from [7]. This is to prove that the analysis can be extended to current starved inverters and also to show the disadvantage of defining jitter in terms of the rms values alone and also to highlight some of the shortcomings of the analysis adopted.

Noise (mV) / Freq (MHz)	10	20	30	40	62.5	70
10	0.002142	0.008629	0.009097	0.01102	0.01492	0.0163
20	0.00446	0.0115	0.01532	0.01811	0.02416	0.0286
30	0.00964	0.01301	0.01902	0.0242	0.0387	0.04048
40	0.00659	0.01273	0.02266	0.02986	0.04577	0.0503
50	0.00769	0.01498	0.02243	0.02894	0.04799	0.05445
60	0.00788	0.01825	0.02139	0.02981	0.0473	0.0561
70	0.00799	0.0157	0.02597	0.03182	0.04972	0.0552

Table 3.3 RMS Cycle-to-Cycle Jitter (ns)

To calculate the rms value, the difference between the consecutive periods was taken and time averaging was performed. The theoretical calculation for the rms value requires the determination of the static sensitivity of the VCO frequency towards DC variation of the power supply. This value can be determined from the following graph between the frequency of the VCO and the supply voltage. The slope of the line represents the sensitivity of the VCO and it was found to be 31.36MHz/V. The calculated values for cycle-to-cycle jitter are as shown in table 3.4.

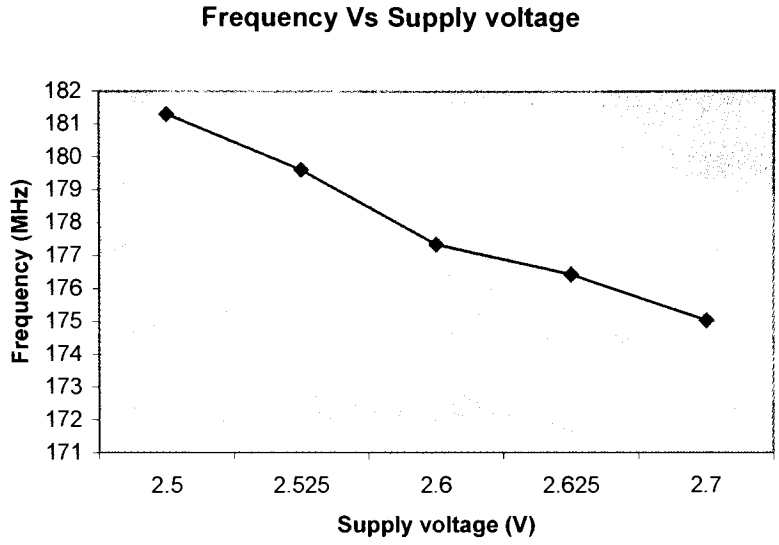


Fig 3.5 Graph of Frequency Vs Supply voltage

Noise (mV) / Freq (MHz)	10	20	30	40	62.5	70
10	0.002337785	0.004675571	0.0070134	0.009351	0.014611	0.016364
20	0.004675571	0.009351141	0.0140267	0.018702	0.029222	0.032729
30	0.007013356	0.014026712	0.0210401	0.028053	0.043833	0.049093
40	0.009351141	0.018702283	0.0280534	0.037405	0.058445	0.065458
50	0.011688927	0.023377853	0.0350668	0.046756	0.073056	0.081822
60	0.014026712	0.028053424	0.0420801	0.056107	0.087667	0.098187
70	0.016364497	0.032728995	0.0490935	0.065458	0.102278	0.114551

Table 3.4 Calculated RMS Cycle-to-Cycle Jitter

From looking at the calculated rms values we arrive at the following conclusions,

1. The calculated rms values match the simulation results until the noise frequency reaches about 40MHz. But, for frequencies above 40MHz we see that the calculated rms value still increases linearly whereas the simulated value has attained a saturation level.

   This means that the validity of the theoretical expression is about $1/6^{th}$ of the operating frequency of the VCO.

2. When we simulated for a noise frequency of 90MHz (half of the operating frequency) with an amplitude of 20mV we found that the rms value was about 9.9ps, which is much lesser than the calculated rms value and the interesting point to note is that the simulated value was much less than the one obtained for noise frequency of 30MHz with the same amplitude.

3.4 Comparison Of Results

The preceding section provided the results obtained from simulations. This section shows the predicted values for maximum cycle jitter and cycle-to-cycle jitter. Before we look at the values for cycle jitter and cycle-to-cycle jitter, it is important to make sure that the transfer function obtained in section 3.2 is able to predict the timing error accurately. The following graph shows the comparison between the cycle-to-cycle jitter values obtained from the simulator in comparison with the values calculated using the transfer function obtained. The noise voltage amplitude was kept at 70mV and the frequency of the signal was 20MHz. The data point of interest for our analysis is the peak value of the cycle-to-cycle jitter.

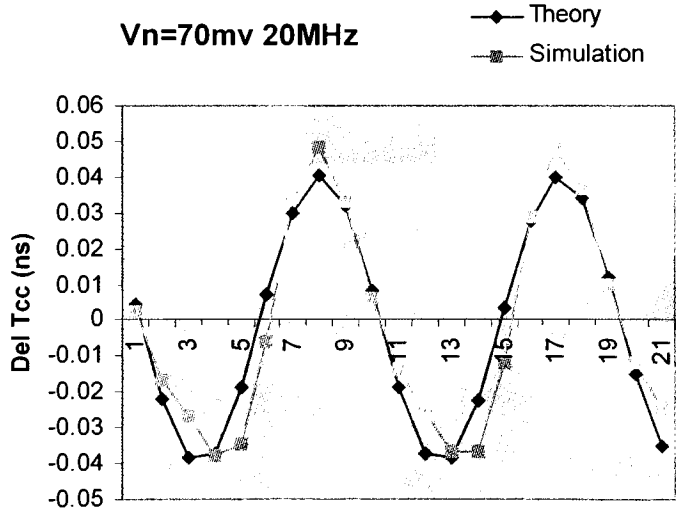


Fig 3.6 Graph of Cycle-to-Cycle Jitter

It is not possible to predict the value of the noise voltage for consecutive period of the VCO. So, the noise voltage values on the power supply were obtained from the simulator and the timing error was calculated using the transfer function obtained.

Table 3.5 has the theoretically predicted values for maximum cycle jitter for different noise voltage combination obtained using the transfer function.

Noise (mV) / Freq (MHz)	10	20	30	40	62.5	70
10	0.00849	0.01698	0.02547	0.03396	0.053076	0.05944
20	0.00849	0.01698	0.02547	0.03396	0.053076	0.05944
30	0.00849	0.01698	0.02547	0.03396	0.053076	0.05944
40	0.00849	0.01698	0.02547	0.03396	0.053076	0.05944
50	0.00764	0.01528	0.02292	0.03057	0.047769	0.053501
60	0.00642	0.01284	0.019260	0.02568	0.040126	0.044941
70	0.00551	0.01104	0.016559	0.02208	0.03449	0.038639

Table 3.5 Predicted Maximum Cycle Jitter (ns)

To compare the results obtained, an example graph is shown below. The noise amplitude in the graph was kept constant at 70mV and the frequency was varied from 10MHz to 70MHz.

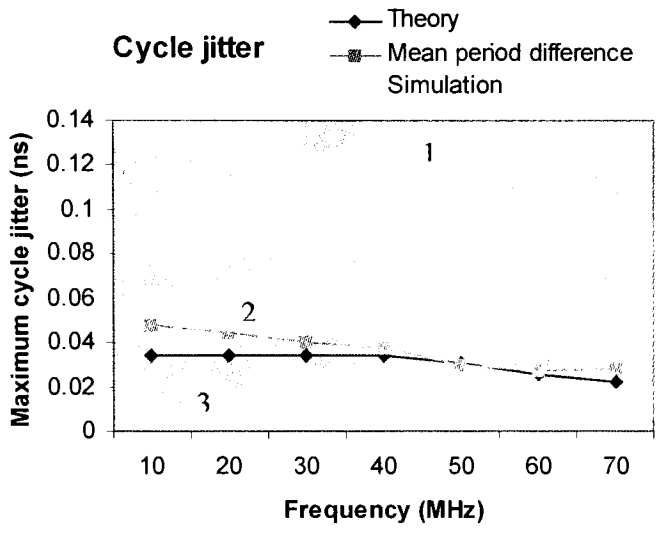


Fig 3.7 Graph of Maximum Cycle Jitter Vs Frequency

The graph shows the comparison between the simulated value and the theoretically predicted value. The line marked "1" shows the simulated result for the cycle jitter. The line marked "2" is the cycle jitter value, when the present period was subtracted from its mean period instead of subtracting it from the period of the VCO. The line marked "3" shows the calculated value for the cycle jitter. The simulated values were found to be greater than the theoretically predicted value and this is because of the inability to predict the exact noise voltage value.

The prediction of cycle jitter is not as accurate as predicting the cycle-to-cycle jitter. This is owing to the deficiency in the analysis adopted. For theoretical calculations, we have made use of the small signal model of the transistors, which calculates the gain offered by the transistor based on the transconductance and output impedance values. For proper determination of cycle jitter we need to predict the effect of a single voltage value on the power supply, which is not possible because the small signal model can predict only the effect of change in the noise voltage ΔV. In the case of cycle-to-cycle jitter, we do not have this problem because, we are calculating the difference between consecutive periods due to the variation of the noise on the power supply and the small signal model is sufficient enough to study the effect of the difference in noise voltage value. But, we still see that the cycle jitter value decreases as the noise signal frequency crosses 40MHz as predicted by the theory. Also, if we compute the cycle jitter by taking the difference of the present period and its own period, then the simulated values match with the predicted value closely.

The second parameter taken for comparison is the cycle-to-cycle jitter of the VCO. The maximum cycle-to-cycle jitter occurs when the difference in the magnitude of the noise on the power supply between consecutive periods is the maximum. To obtain this value, the ratio of the frequency of the noise signal to the normal VCO frequency is used. An example calculation for the noise voltage magnitude is shown here.

Assume the noise signal frequency is 70MHz (approximately 14.285ns). The time the signal takes to change from one peak value to the other is then about 7.2ns. To calculate the noise voltage to which the VCO is exposed, we take the ratio of 7.2ns to the time period of the VCO. In this case the ratio is 1.3. The corresponding voltage is then the peak-peak value divided by the ratio obtained earlier. For example, the noise amplitude of 10mV will have a maximum voltage swing of 15.4mV between two consecutive periods. Using this voltage value and the first crossing theory, the timing error can be calculated. By following the same method we can determine the voltage values for each frequency and amplitude value. The table shows the theoretically predicted values for the jitter.

Noise (mV) / Freq (MHz)	10	20	30	40	62.5	70
10	0.002548	0.004586	0.006879	0.009172	0.013588	0.015286
20	0.004586	0.009172	0.013758	0.018343	0.027175	0.030572
30	0.006879	0.013758	0.020382	0.027515	0.040763	0.045858
40	0.009172	0.018343	0.027175	0.036687	0.054351	0.061145
50	0.011465	0.022929	0.034394	0.045858	0.067938	0.076431
60	0.012738	0.025477	0.038215	0.050954	0.081526	0.091717
70	0.014437	0.028874	0.043311	0.057748	0.090868	0.107003

Table 3.6 Predicted Maximum Cycle-to-Cycle Jitter (ns)

The interesting point to note from the obtained values for cycle-to-cycle jitter is that there is a line of symmetry along the diagonal. The reason for the symmetry is because the slope of the noise signal is the same on either side of the diagonal. For example, a noise amplitude of 20mV with frequency of 10MHz will have the same slope as a noise signal with amplitude of 10mV with associated frequency of 20MHz. So by theory, the maximum cycle-to-cycle jitter values will be the same for two different noise signals if the ratios of their amplitudes and their frequencies are inverse of each other.

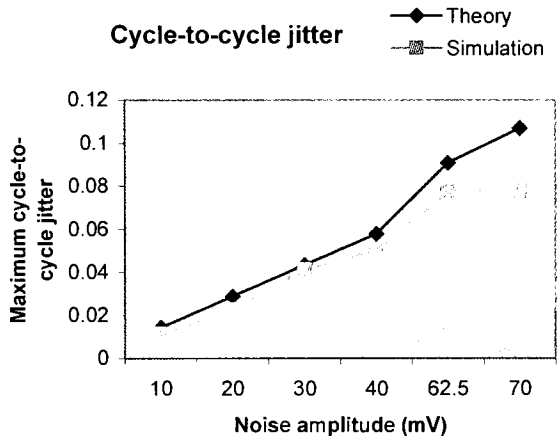


Fig 3.8 Graph of Maximum Cycle-to-Cycle Jitter Vs Noise Amplitude

The maximum cycle-to-cycle jitter value shown in the graph is for noise frequency of 70MHz. The theoretical value matches well with the simulated result when the noise amplitude is less than 70mV. But, for higher values, the theory still predicts a linear increase whereas the simulated result does not have a linear

increase. The reason for this is, the circuit is not able to adapt to such fast changes in the noise magnitude on the power supply and it starts slewing. The other reason is the large amplitude of the noise signal. The small signal model is based on the assumption that the input voltage does not affect any other bias conditions. If this condition is not satisfied, then the gain or the transfer function predicted will be different from what the simulator calculates. It was found from the simulator that the transfer function was less for noise amplitude of 70mV when compared with the other lesser noise amplitude values.

Chapter 4

Analysis of Effect of Substrate Coupling noise

The other major noise source affecting the performance of the VCO in terms of the timing error is the noise due to substrate coupling effect. The following chapter involves the analysis of the jitter caused due to this noise source. It is important to understand the noise mechanism and to know why it is important to study the effect of the noise. The theoretical analysis along with the calculation of the noise voltage caused due to the noise is presented in this section. The second section contains the simulation results, which has details about the maximum cycle jitter and maximum cycle-to-cycle jitter of the VCO. A comparison between the theoretical prediction and the simulated result is presented in Section 3. Finally, an attempt has been made to study the effect of the two noise sources on the jitter when they are present simultaneously is studied and results obtained for the jitter are presented here.

The chip layout for the designed VCO is given as part of this chapter. The section contains details as to how the chip needs to be designed so that testing of the VCO for jitter can be performed.

4.1 Substrate Noise Mechanism

The main source for substrate noise is the digital component in large mixed signal integrated circuits. In mixed signal IC's, the digital components and the analog components normally share the same substrate. Fast switching digital signals send current spikes into the substrate and this propagates along the substrate to affect sensitive analog circuits.. The substrate noise gets coupled to the transistor due to the presence of the parasitic capacitance such as C_{bd} and C_{bs}. The variation in the substrate voltage affects the threshold voltage and therefore degrades the performance of the analog circuitry. The effect of substrate noise is felt more in the NMOS transistors, which are placed in the p-substrate, whereas the PMOS transistors are placed in a n-well, which reduces the impact of the substrate coupling effect. Various mechanisms have been designed to reduce the severity of the effect of substrate noise, like having guard rings, which are basically heavily doped wells surrounding sensitive analog circuits. The doped well acts as a shield for the sensitive circuitry.

With increasing complexity of on-chip circuitry and with increase in the number of digital components that are switching, the study of effect of substrate noise on sensitive circuits like the VCO is very important.

4.1.1 Determination of transfer function

The following analysis is done in order to relate the noise due to the substrate coupling effect to the jitter of the VCO. To achieve this, we need to determine the output voltage deviation caused by variation of the body voltage. The variation of the bulk potential or the body voltage influences the threshold voltage and hence the gate-source overdrive. As a result of the threshold voltage variation, the charging and discharging current are different. This variation of threshold effect is called the "body effect" or the "backgate effect". The variation of threshold voltage and its dependence on the body voltage can be understood from the following expression [15].

$$V_{th} = V_{tho} + \gamma(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}) \qquad (4.1)$$

where V_{th} represents the threshold voltage at the given bias condition, V_{tho} represents the native threshold voltage, Φ_F is the fermi potential, V_{SB} is the source-bulk potential difference, γ denotes the body effect co-efficient and is given by

$$\gamma = \sqrt{2q\varepsilon_{si}N_{sub}}/C_{ox} \qquad (4.2)$$

Typically, the value of γ is in the range of $0.5V^{1/2}$.

The output voltage deviation can be related to the variation of the body bias in terms of a parameter called g_{mbs}, which represents the body-source small signal transconductance. The following figure (fig 4.1) shows the small signal model of a MOS transistor with a dependent current source representing the body effect.

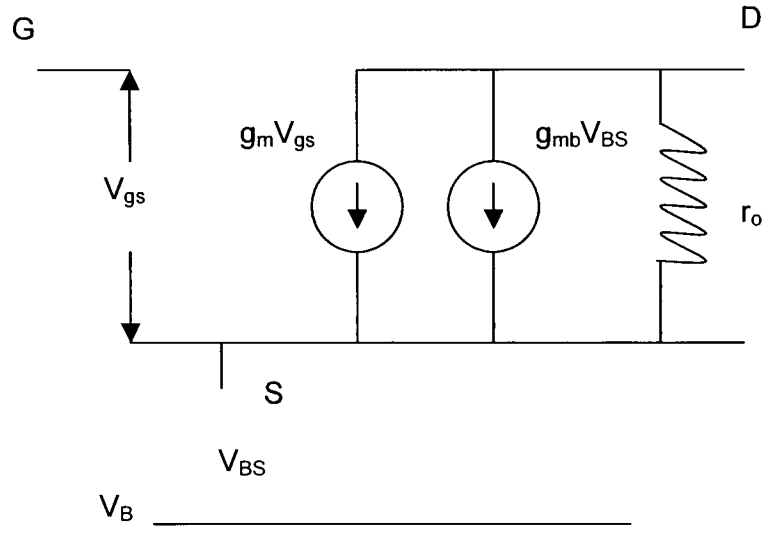


Fig 4.1 Small Signal Model with body effect represented by dependent current source

Even though the reason for studying the variation of the body voltage is due to the dependence of threshold voltage, the simulator calculates the threshold voltage as a DC function and therefore the simulator fixes the threshold voltage for each of the transistors. So, the output voltage variation of a VCO due to the body effect can be studied using this dependent current source in the MOS model.

The analysis is similar to that adopted to study the effect of power supply noise. Single stage of the inverter is used to determine the deviation of the output voltage due to variation of the body voltage. The main contributor to the noise voltage is the bias network. The reason for this is, even a small variation in the current in the bias network is magnified by the ratio of the transistor in the current starved network to the size of the transistor in the bias network. The noise effect due to substrate coupling is studied only in NMOS transistors. The reason being, in a typical n-well process, the PMOS transistors are placed in a highly doped n-well. As a result, the propagation of substrate noise and its subsequent effect on the operation of the PMOS transistor is relatively less. For NMOS transistors, as bulk voltage is reduced, V_{SB} increases and hence the threshold voltage increases and vice versa.

The contribution of the bias network to the noise voltage can be calculated as follows:

Bias Network: The bias network has two NMOS transistors that contribute to noise. The deviation of the current due to variation of the body voltage is given by

$$\Delta I_b = (g_{mbs1} + g_{mbs2}) * \Delta V_b \qquad (4.3)$$

where ΔI_b is the variation of the bias current, g_{mbs1} and g_{mbs2} are the small signal body to source transconductance and ΔV_b is variation of the body voltage.

The variation of current in the current starved network is obtained by multiplying the above expression with ratio of the size of the PMOS transistor in the current starved network to the size of the bias transistor. The reason for this is, the time period of the output is measured when the load capacitance is being charged, which is controlled by the PMOS current. Therefore, any variation in the PMOS current will cause the time period to be different.

$$\Delta I = \Delta I_b * S_P / S_b \qquad (4.4)$$

where ΔI is the variation of current in the current starved network, S_p and S_b represent the size of the transistors.

First Stage:

The first stage contributes to the noise voltage due to the presence of the two NMOS transistors in the current starved network. The variation of current due to these two transistors is given by

$$\Delta I_1 = (g_{mb3}+g_{mb4}) * \Delta V_{bs} \qquad (4.5)$$

where g_{mb3}, and g_{mb4} are the body-source transconductance and ΔV_{bs} is variation in the body source voltage.

The total deviation of current is given by the sum of eqn. (4.5) and eqn (4.4). The deviation in the output voltage is then the product of the deviation in output current and the net output resistance. The output resistance expression has already been derived as part of the previous chapter and it is given by the following expression.

$$R_0 = \{[1+ g_{m2} r_{02}]^* r_{01}+ r_{02}\} \parallel \{[1+ g_{m3} r_{03}]^* r_{04}+ r_{03}\} \qquad (4.6)$$

The deviation in the output voltage due to the variation in the current is then given by

$$\Delta V_0 = \Delta I_t * R_0 \qquad (4.7)$$

where ΔV_0 is the deviation in the output voltage of the inverter, ΔI_t is the total deviation in the output current and R_0 is the output resistance.

Second stage:

For estimating the noise voltage magnitude at the output of the second stage, we need to study the inter-stage correlation effect between the output of the first stage and the second stage. As calculated in the previous section, the transfer function between the output of the inverter and the input noise voltage is

$$V_{0p}/V_{in} = g_{mp}*R_0 \text{ and } V_{0n}/V_{in} = g_{mn}*R_0 \qquad (4.8)$$

$$V_{02} = (V_{0p} + V_{0n})*V_{in} \qquad (4.9)$$

where V_{02} is the contribution of output noise voltage due to input noise, V_{0p} and V_{0n} are the output noise voltage due to the PMOS and NMOS transistors respectively, g_{mp} and g_{mn} are the transconductance of the transistors, R_0 is the effective output resistance at the output of the inverter, and V_{in} represents the magnitude of noise voltage at the input of the transistor. For the second stage, V_{in} represents the gain provided by the first stage, which is the transfer function derived in equation (4.7).

The objective is to obtain the transfer function between the noise on the body contact and the output voltage deviation. The gain provided by the input transistors are opposite in phase with respect to the gain offered by the current starved network and the bias network combined. The effective transfer function will be the difference between the individual values.

$$TF_2 = \Delta V_{02}/\Delta V_b = V_{02} - TF_b \qquad (4.10)$$

where TF_2 is the transfer function between the output of the second stage and body voltage variation, and TF_b is the transfer function between the noise on the

4.1.2 Calculation of noise voltage

The noise voltage at the output of each of the inverter can be calculated using the equations derived in the previous section. The biasing conditions are the same as for the power supply noise analysis and hence, the drain current and transconductance values are the same as before. The relation between the body-source transconductance and the transconductance of the transistor is given by

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}} \qquad (4.13)$$

where g_{mb} is the body-source transconductance, g_m is the transconductance, γ is the body effect co-efficient and Φ_F represents the fermi potential.

$$\Phi_F = \Phi_t \ln\left|\frac{N_A}{n_i}\right| = 0.456V \qquad (4.14)$$

$$2\Phi_F = 0.9122V$$

The body effect co-efficient is obtained from the MOSIS model file and it was found to be $0.52V^{1/2}$. Using these values and the transconductance values for the respective transistors, the body-source transconductance values for the NMOS transistors were obtained and are as shown in the following table.

Transistor	g_{mbs} (S)
M1	6.177e-6
M2	2.8707e-6
M3	0.000158
M4	0.000624

Table 4.1 Body-Source Transconductance values for the NMOS transistors

The effective resistance at the output of the inverter is the same as found before and is equal to 701.2Ω.

The contribution of the bias network towards the noise voltage was found to be

$$\Delta V/\Delta V_{bs} = (g_{mbs1}+g_{mbs2})*R_0*S_p/S_b = (6.177e\text{-}6+2.8707e\text{-}6)*701.2*1000 = \mathbf{6.3442}$$

The noise voltage due to the NMOS transistors in the first stage is given by

$$\Delta V_1/\Delta V_{bs} = (g_{mb3}+g_{mb4})*R_0 = (0.000624+0.000158)*701.2 = \mathbf{0.549}$$

Therefore, the effective voltage deviation at the output of the first stage of the inverter is given by

$$\Delta V_{01} / \Delta V_{bs} = 6.3442+0.549=\mathbf{7.001}$$

Second stage:

The transfer function between the variation of the bulk potential and the output voltage deviation is given by

$$TF_2 = \Delta V_{02}/\Delta V_b = V_{02} - TF_b = (7.001*1.44114) - 7.001 = \mathbf{3.0884}$$

Third stage:

Here, the gain provided by the inverter to the bulk potential variation and the gain provided by the input transistors are in phase. The transfer function between the input and output of the inverter is the same as that for the second stage. The final transfer function between the variation of the bulk potential and the voltage deviation is

$$TF_3 = \Delta V_{03}/\Delta V_b = V_{03} + TF_b = (3.0884*1.44114)+7.001 = \mathbf{11.452}$$

The final transfer function relating the noise voltage variation and the output voltage deviation in terms of the individual stages is given by

$$\Delta V_0/\Delta V_b = (TF_1+TF_3)^* \Delta V_b - TF_2^* \Delta V_b$$

$$= \mathbf{18.453^* \Delta V_b - 3.0884^* \Delta V_b}$$

The reason why we have the negative sign in the above equation is because, when the first and the third stage are in the charging period, the second stage is in the discharging period and vice versa, and the slew rate is different between the charging and discharging period. As a result, the timing error needs to be calculated separately. The timing error is given by

$$\mathbf{\Delta t = 18.453^* \Delta V_b /SR_c - 3.0884^* \Delta V_b/SR_d}$$

where SR_c and SR_d are the slew rate corresponding to the charging and discharging period of the output.

4.2 Simulation results

This section has details about the simulations performed in order to determine the maximum cycle jitter and maximum cycle-to-cycle jitter for the VCO caused due to the variation of the bulk potential. The schematic (fig 4.2) shows the simulation setup wherein a noise source has been connected to the body contacts of the NMOS transistors.

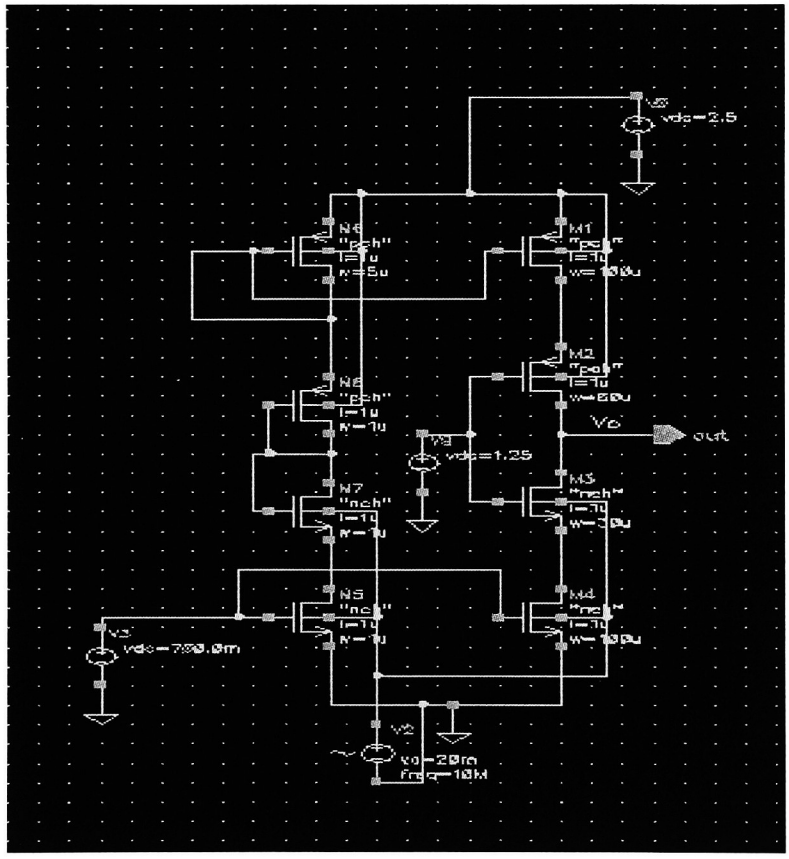


Fig 4.2 Single Stage showing noise voltage on the body contact

The noise amplitude was varied from 10mV to 50mV and the noise frequency was varied from 10MHz to 50MHz. The reason for not simulating for higher amplitude and frequency values was because the obtained cycle and cycle-to-cycle jitter were nearly 50% of the rise time for a noise signal with amplitude of 50mV and frequency of 50MHz.

The following table shows the simulated values obtained for maximum cycle-to-cycle jitter. To obtain these values, the difference between the present period and the preceding period was taken and the maximum value of jitter for each noise voltage combination has been tabulated.

Noise (mV) / Freq (MHz)	10	20	30	40	50
10	0.02197	0.05311	0.07574	0.08871	0.10941
20	0.0425	0.09281	0.13158	0.17137	0.20808
30	0.06909	0.09914	0.17341	0.2343	0.3025
40	0.07817	0.15444	0.23161	0.30613	0.3676
50	0.09145	0.1834	0.26045	0.34667	0.43271

Table 4.2 Maximum Cycle-to-Cycle Jitter (ns)

The other parameter of interest is the cycle jitter. With similar noise signal combinations, the simulations were performed and the cycle jitter was calculated by taking the difference between the present period and the mean period of the VCO. The maximum cycle jitter obtained are as shown in the following table. The values shown in both the tables represent the magnitude of the timing error.

Noise (mV) / Freq (MHz)	10	20	30	40	50
10	0.07005	0.20848	0.24271	0.30734	0.35978
20	0.0668	0.20376	0.2526	0.30255	0.35103
30	0.14127	0.19586	0.22623	0.3002	0.35655
40	0.06202	0.19676	0.24388	0.28893	0.3476
50	0.06662	0.18963	0.24024	0.29934	0.34949

Table 4.3 Maximum Cycle Jitter (ns)

4.3 Comparison Of Results

To make sure that the transfer function calculated is capable of predicting the jitter, the following graph was plotted. The body voltage variation taken from the simulator was used to calculate the timing error between two consecutive periods or the cycle-to-cycle jitter. This value was plotted against the time period difference obtained from the simulator. The noise signal amplitude was 10mV and the frequency was set to 20MHz.

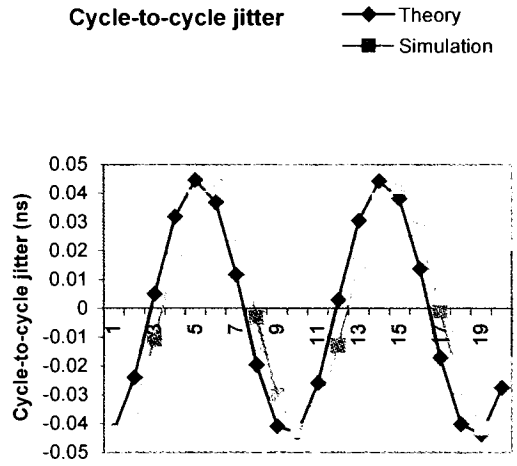


Fig 4.3 Graph of Cycle-to-Cycle Jitter

We can see from the graph that the theoretical value matches well with the simulated value. The data points of interest in the above graph are the peak

values of the cycle-to-cycle jitter, which represent the maximum cycle-to-cycle jitter for that particular noise voltage.

The timing error due to the noise signal was predicted theoretically using the transfer function derived in section 4.1. For predicting these values, the definition for maximum cycle jitter and cycle-to-cycle jitter as derived in the previous chapter was used. Therefore, the noise voltage variations causing the maximum timing error are the same as that derived before, but the transfer function used to calculate the timing error is different. The maximum cycle-to-cycle jitter due to the noise signal predicted by the theory are as shown in the following table. We can see that the jitter increases linearly as we increase either the frequency keeping the amplitude constant or vice versa.

Noise (mV) / Freq (MHz)	10	20	30	40	50
10	0.019811	0.035661	0.053491	0.071321	0.089151
20	0.035661	0.071321	0.106982	0.142642	0.178303
30	0.053491	0.106982	0.158491	0.213963	0.267454
40	0.071321	0.142642	0.211322	0.285284	0.356605
50	0.089151	0.178303	0.267454	0.356605	0.445757

Table 4.4 Predicted Maximum Cycle-to-Cycle jitter (ns)

An example graph to show how well the theory matches with the simulated result is given below.

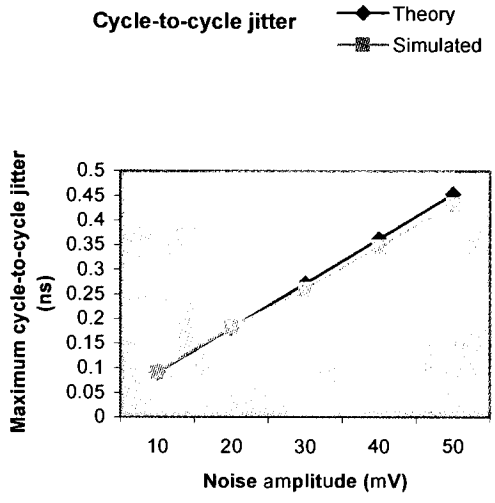


Fig 4.4 Graph of Maximum Cycle-to-Cycle Jitter Vs Noise Amplitude

In the above graph, the noise amplitude was varied from 10mV to 50mV and the noise frequency was kept constant at 50MHz. The peak jitter increased linearly as predicted by the theory. Similar behavior was found for other noise frequencies used for simulations. The reason for this linear increase is because, the slope of the signal increases as the frequency increases and therefore the noise voltage variation between two consecutive periods of the VCO will also increase. As a result of this, the timing error between two consecutive periods also increases, as determined by the transfer function.

Here also we can see the line of symmetry along the diagonal. The reason is because on either side of the diagonal, the slopes of the noise signal are the same and hence, the noise signal variations are also the same. Therefore, the timing error caused due to these noise signal combinations will also be the same.

The maximum cycle jitter predicted by the theory is as shown in the table

Noise (mV) / Freq (MHz)	10	20	30	40	50
10	0.0660	0.13207	0.1981	0.2641	0.3301
20	0.0660	0.13207	0.1981	0.2641	0.3301
30	0.0660	0.13207	0.1981	0.2641	0.3301
40	0.0660	0.13207	0.1981	0.2641	0.3301
50	0.05943	0.11886	0.17830	0.2377	0.29717

Table 4.5 Predicted Maximum Cycle Jitter (ns)

The maximum cycle jitter is constant for a particular amplitude value till the noise frequency is less than 45MHz ($1/4^{th}$ of operating frequency), after which the maximum cycle jitter starts rolling off. The reason for this is, for higher frequencies (greater than $1/4^{th}$), the magnitude of the noise voltage to which the VCO is exposed is lesser than that for lower frequencies.

The comparison between the theoretical prediction and the simulated results are discussed using the following graph.

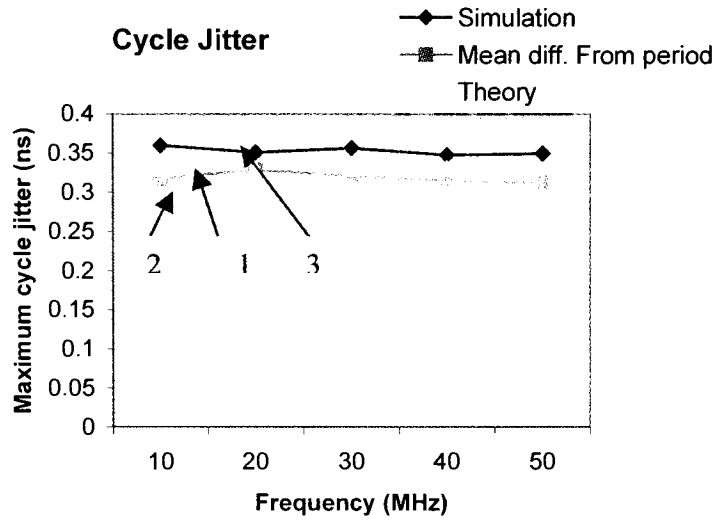


Fig 4.5 Graph of Maximum Cycle Jitter Vs Frequency

The noise signal amplitude was kept constant at 50mV for the above graph. The plot marked "1" in the above graph represents the simulated values obtained for the corresponding noise frequency. The plot marked "2" is the value of the timing error when the present period was subtracted from its own mean period. The line marked "3" is the value of cycle jitter predicted by the theory. The theoretical value is less than the simulated value even though it matched well with plot number "2". The reason is, for theoretical calculations we have made

the noise source and the timing error can be represented as the sum total of the individual contributions towards the timing error and it is given by

$$\Delta t = (18.453^* \Delta V_b + 2.4392 \Delta V_{DD}) / SR_c - (3.0884^* \Delta V_b + 0.40826 \Delta V_{DD}) / SR_d$$

where ΔV_b and ΔV_{DD} are the noise voltage variation on the body contact and on the power supply, SR_c and SR_d represent the slew rate during the charging and discharging of the output.

Using the above transfer function, estimation can be made as to what the magnitude of the maximum timing error will be due to the presence of the two noise sources. The simulations were performed when the two noise sources were out of phase. The reason is, the effects of the two noise sources are opposing each other and therefore, a study of the worst case in terms of the timing error had to be done.

For the first set of simulations, the power supply noise was kept at constant amplitude of 20mV and frequency of 30MHz. The amplitude of the noise voltage on the body contact was also kept at 20mV, but the frequency was varied from 10MHz to 50MHz. The following graph shows the plot of the maximum cycle-to-cycle jitter obtained from the simulations and the calculated maximum jitter.

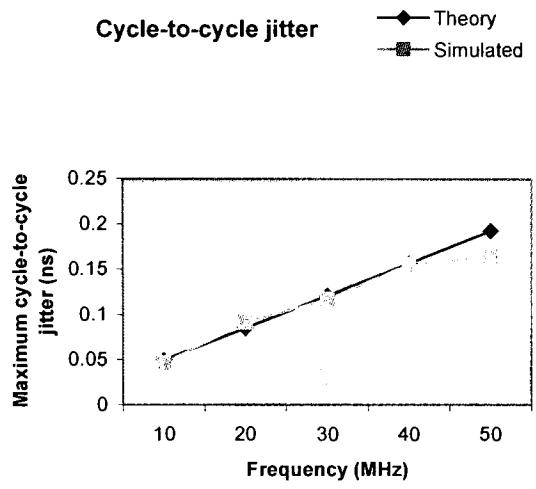


Fig 4.6 Graph of Maximum Cycle-to-Cycle Jitter Vs Frequency

It can be seen from the graph that the theoretical value matches well with the simulated result till about 40MHz.

In the next set of simulation, the noise amplitude on the body contact was kept constant at 20mV and 30MHz and the noise on the power supply was varied. The following graph shows the plot of the maximum cycle-to-cycle jitter obtained from simulations as compared with the theoretical value.

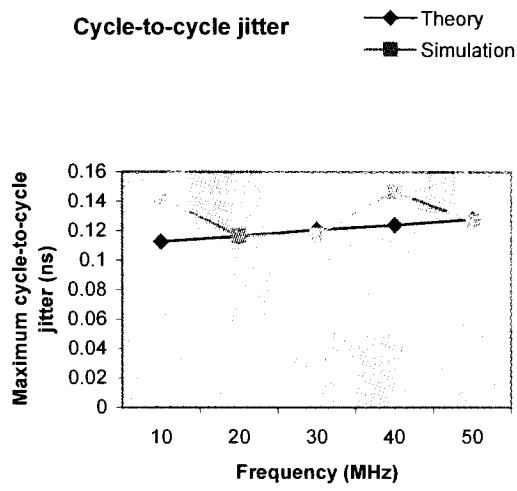


Fig 4.7 Graph of Maximum Cycle-to-Cycle Jitter Vs Frequency

The maximum error between the calculated and simulated value was about 30ps at noise frequency of 10MHz. Otherwise, the values matches well. Another point to note is the magnitude of the jitter. The maximum cycle-to-cycle jitter in the previous case went upto 0.2ns, whereas here the maximum cycle-to-cycle jitter is around 0.15ns. This means that the effect of substrate noise is more on jitter than the effect of power supply noise for the same noise signal combination.

4.5 Chip Layout

The layout for the VCO was done using Virtuoso layout editor, provided with the Cadence suite. The layout is shown in figure 4.8. The jitter of the VCO due to each of the noise sources needs to be measured. To inject noise on the power supply, the existing V_{DD} connection can be used. The noise can be superimposed on the DC power supply. But, to study the substrate coupling effect, we need to have diffusion where we can inject noise. The diffusions need to be placed on the p-substrate. The noise injected using this diffusion would affect the body contacts that are normally placed to bias the p-substrate. Diffusion contact at different distances from the NMOS transistors can be placed if we need to model the substrate noise propagation mechanism.

The chip size was 180µ*180µ. The biasing PMOS transistors occupy most of the chip area, because of their large sizes when compared with the other transistors. The biasing of the n-well and the p-substrate is very important. Otherwise, it may so happen that the Source-Body junction or the Source-Drain junction might be forward biased.

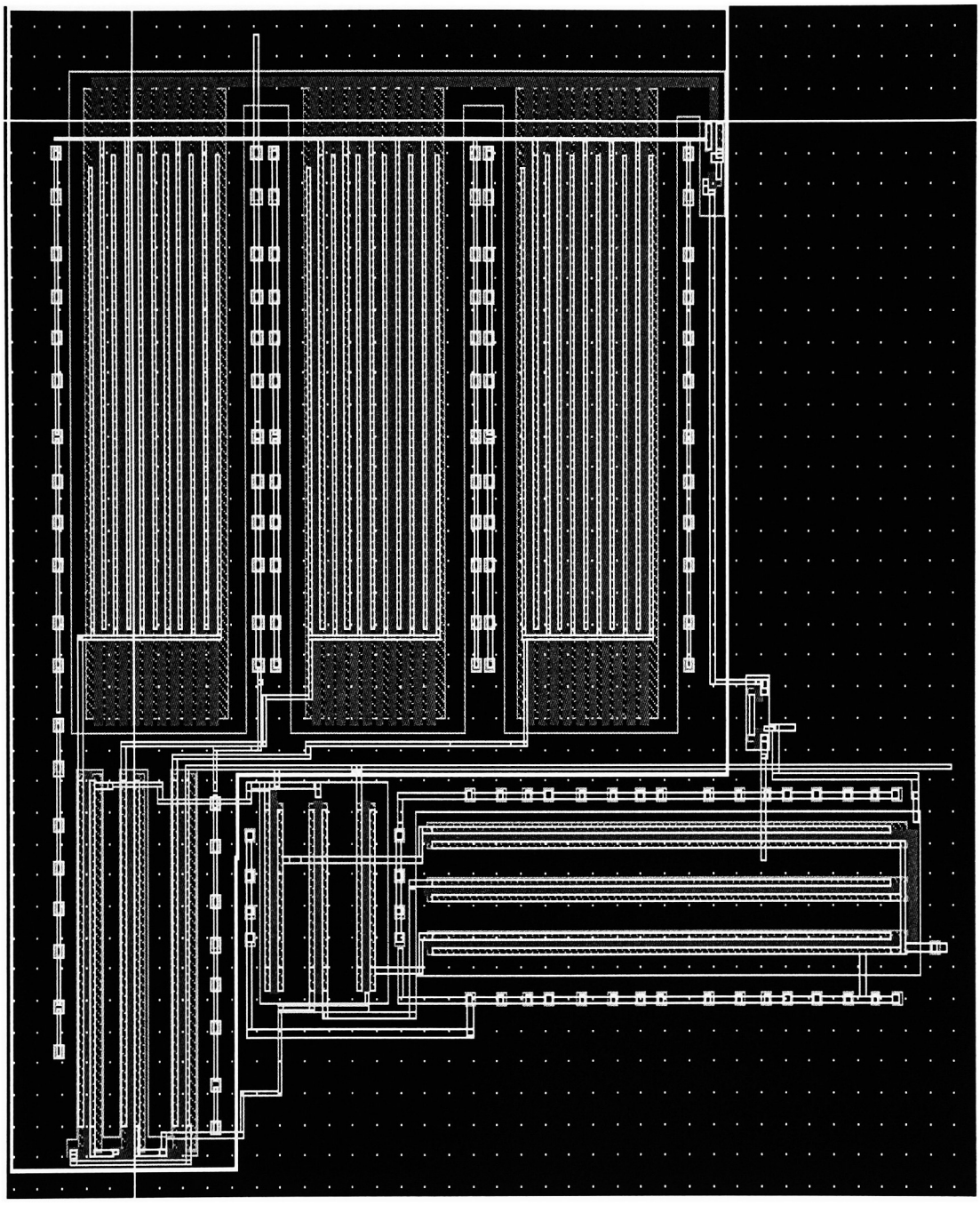


Fig 4.8 VCO Layout

Chapter 5

Conclusion

The performance of a PLL is greatly influenced by the performance of the VCO. The timing error or phase noise of the VCO is the most important non-ideality. It is important to understand the effect of the noise sources on the timing error or jitter. Even though there has been research in this field, previous work has not tried to use the circuit parameters to relate the noise and the timing error. Once a relation is obtained, a qualitative analysis can be adopted in order to come up with a VCO design, whose sensitivity to noise in terms of timing error is lesser. Also, peak jitter is a much better parameter to define the performance of a VCO then the rms value, because only the peak jitter determines the data transfer rate in digital applications whereas the rms jitter only gives an average of the timing error, which is not much of interest in design issues.

This thesis is aimed at studying the effect of two main noise sources namely the noise on the PDS and the noise due to substrate coupling effects on the jitter. The objective is to relate the error to design parameters like transconductance and output resistance of the transistors. From the results shown, we can conclude that the theory is able to predict to a certain amount of accuracy as to what the timing error will be.

The main contributions of the thesis presented here are

1. The analysis presented here is scalable, which means that it is not specific to a particular frequency of the VCO or the noise signal. The analysis can be extended to any VCO design operating at any frequency.

2. It is not always the high frequency noise that affects the VCO. For example, in one of the test cases for the power supply noise analysis, the amplitude was kept constant and the frequency was varied from 10MHz to 180MHz (equal to the VCO frequency), it was found that the cycle-to-cycle jitter started decreasing after 90MHz and for noise frequency of 180MHz the maximum cycle-to-cycle jitter was 0.9ps. This is as predicted by the theory. Similar argument can be made for the substrate coupling effect as well.

   By applying the scalable property, it can be said that, if the VCO frequency is f_0, then the maximum cycle-to-cycle jitter will start reducing after the noise frequency crosses $f_0/2$ and this continues till the noise frequency reaches f_0. A plot of the jitter against the noise frequency will resemble a sine wave.

3. The contribution of substrate noise towards jitter is about "9" times more than the power supply noise contribution for the same noise signal combination.

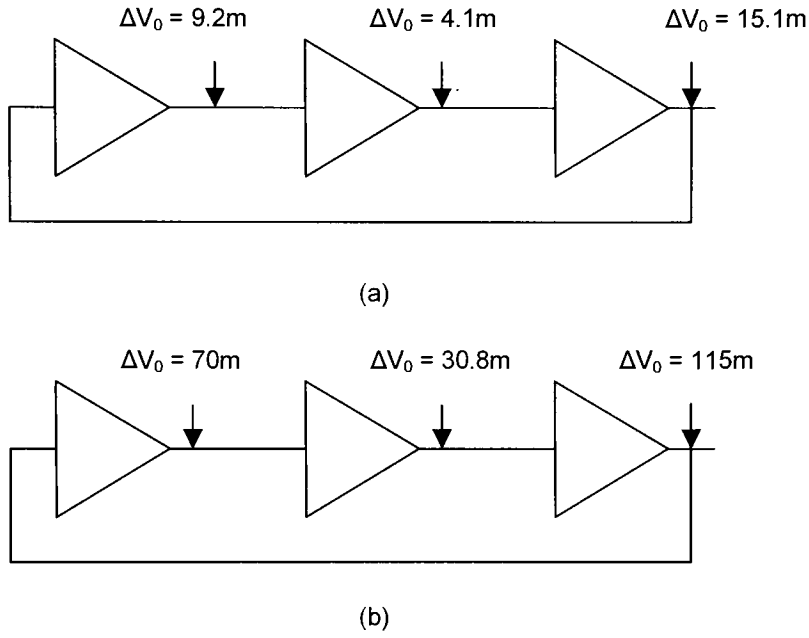


Fig. 5.1 Noise Voltage Deviation (a) Noise on Power Supply (b) Substrate Coupling Noise

The figure is an illustration of the noise voltage at the output of each stage of the inverter. It is an example case wherein we have noise voltage amplitude of 10mV on either the power supply or the body contact depending on the case. The timing error ratio will be the ratio of the noise voltage deviation.

But, it is very difficult to determine the exact magnitude of the substrate noise that is affecting the transistors. The reason is, it is very difficult to model the substrate and study the propagation of noise in it, whereas in the power supply case, a profile of the noise voltage across the board can be obtained from an EM field solver.

If there is a specification for the maximum allowable jitter, then as a designer, an allocation can be made between the maximum allowable power supply noise and substrate noise and controlling techniques can be used to make sure that the noise voltage does not exceed the limit.

4. It is important to characterize the jitter in terms of the maximum deviation from the mean period and it is not sufficient to know the rms timing error.

Future Work

The analysis presented takes into account the noise on the PDS and the noise due to substrate coupling effect. But, there are other noise sources, which affect the performance of the VCO, such as the thermal noise due to transistors and the low-frequency noise or 1/f noise. So the next step would be to combine the effect of these sources along with the already derived expressions.

From the analysis presented here and with jitter specification of the VCO, we can come up with an allowable noise margin for the VCO. Based on this noise margin, a placement methodology for the chip can be developed so that the circuit confirms to design specifications.

Also, a test chip has been designed and after it is fabricated, measurements can be taken. This would enable us to compare the simulation results, the theoretical results and the measured results.

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```
// TT : typical model for 2.5V Nominal Vt devices
// 2)HDIF depends on your layout poly spacer to contact center distance.
//   The value listed here is TSMC minimum-rule value. you can change it
//   according to your layout.
//
//
// ************************************************************
//                                                  *
//            2.5V NOMINAL Vt DEVICES LIB                  *
//                                                  *
// ************************************************************
// ********** CORNER_LIB OF TYPICAL MODEL ******************
library tsmclib

section tt
parameters toxp=5.4e-9
parameters toxn=5.4e-9
parameters dxl=0
parameters dxw=0
parameters dvthn=0.0
parameters dvthp=0.00
parameters cjn=1.836615e-03
parameters cjp=1.833935e-03
parameters cjswn=4.234822e-10
parameters cjswp=3.472876e-10
parameters cgon=1.3e-10
parameters cgop=1.6e-10
parameters cgln=2.1e-10
parameters cglp=2.1e-10
parameters cjgaten=3.286035e-10
parameters cjgatep=2.500235e-10
parameters hdifn=2.625e-07
parameters hdifp=2.625e-7
include "mix025_1.scs" section=mos
endsection tt

//              NMOS DEVICES MODEL                    *
// ************************************************************
model nch bsim3v3  {
    1: type=n minr=1e-60 lmin=1.2e-06 - dxl lmax=2.1e-05 wmin=1.2e-06
+   dxw wmax=1.01e-04 tnom=25 xl=3e-08 + dxl flkmod=1 af=0.8824 kf=3.454e-
24 xw=0
+ + dxw version=3.2 tox=toxn xj=1e-07 nch=1.63e+17 lln=1 lwn=1 wln=1 wwn=1
lint=2e-08
```

+ wint=2e-08 mobmod=1 binunit=2 dwg=0 dwb=0 vth0=0.4767749 + dvthn lvth0=3.507137e-08
+ wvth0=-1.453229e-08 pvth0=-6.620086e-15 k1=0.4472964 lk1=-5.39693e-08 wk1=-4.269873e-08
+ pk1=5.981896e-14 k2=0.004538423 lk2=2.041006e-08 wk2=1.682965e-08 pk2=-2.784819e-14
+ k3=0 dvt0=0 dvt1=0 dvt2=0 dvt0w=0 dvt1w=0 dvt2w=0 nlx=0 w0=0 k3b=0 vsat=120633
+ lvsat=-0.01265326 ua=-9.218065e-10 lua=-1.161761e-16 wua=1.451009e-16 pua=-5.566174e-23
+ ub=1.81497e-18 lub=1.561614e-25 wub=-2.338524e-25 pub=8.58042e-33 uc=4.365745e-11
+ luc=8.007525e-18 wuc=-7.436576e-18 puc=-6.149303e-24 rdsw=187 prwb=0 prwg=0 wr=1
+ u0=0.03077917 lu0=5.598957e-11 wu0=-8.158919e-11 pu0=1.090017e-15 a0=0.5252816
+ la0=4.042826e-08 wa0=1.225374e-07 pa0=-2.063631e-13 keta=0.003461425 lketa=-9.223886e-09
+ wketa=-8.366612e-11 pketa=1.672486e-15 a1=0 a2=0.65 ags=0.01 b0=0 b1=0 voff=-0.1517445
+ lvoff=2.086556e-08 wvoff=6.482217e-09 pvoff=-7.791971e-15 nfactor=1 cit=0.000377699
+ lcit=7.405382e-10 wcit=-6.34899e-10 pcit=7.555298e-16 cdsc=0 cdscb=0 cdscd=0 eta0=3.836953e-05
+ leta0=2.324929e-10 weta0=8.055062e-12 peta0=-1.610206e-16 etab=-4.68351e-05 letab=-6.326623e-11
+ dsub=0 pclm=0.4755805 lpclm=4.88145e-07 wpclm=-6.231367e-09 ppclm=1.245653e-13
+ pdiblc1=1e-05 pdiblc2=0.0002151594 lpdiblc2=5.69396e-09 pdiblcb=0.01 drout=0 pscbe1=1.213673e+08
+ lpscbe1=265.5531 wpscbe1=-3.167115 ppscbe1=-1.324478e-05 pscbe2=1e-06 pvag=0 delta=0.01
+ alpha0=0 beta0=20.54463 kt1=-0.2402984 lkt1=-1.511487e-08 wkt1=1.116811e-08 pkt1=-1.329005e-14
+ kt2=-0.02232689 lkt2=-1.527194e-08 wkt2=-1.12105e-08 pkt2=1.287179e-14 at=35000
+ ute=-1.688541 lute=3.778586e-09 wute=1.029916e-07 pute=-5.895606e-14 ua1=9.999999e-11
+ ub1=0 uc1=-4.534566e-11 luc1=7.638851e-17 wuc1=8.059368e-17 puc1=-8.934457e-23
+ kt1l=0 prt=0 cj=cjn mj=0.4708251 pb=0.9597901 cjsw=cjswn mjsw=0.379613 pbsw=0.9597901
+ cjswg=cjgaten mjswg=0.379613 pbswg=0.9597901 tcj=0.0007391288 tcjsw=0.0009081566

Appendix B

Parameter Definition [12]

DC Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
K2	k2	Second order body effect coefficient	0.0	none	nl-2
K3	k3	Narrow width coefficient	80.0	none	
K3b	k3b	Body effect coefficient of k3	0.0	1/V	
W0	w0	Narrow width parameter	2.5e-6	m	
Nlx	nlx	Lateral non-uniform doping parameter	1.74e-7	m	
Vbm	vbm	Maximum applied body bias in Vth calculation	-3.0	V	
Dvt0	dvt0	first coefficient of short-channel effect on Vth	2.2	none	
Dvt1	dvt1	Second coefficient of short-channel effect on Vth	0.53	none	
Dvt2	dvt2	Body-bias coefficient of short-channel effect on Vth	-0.032	1/V	
Dvt0w	dvt0w	First coefficient of narrow width effect on Vth for small channel length	0	1/m	
Dvt1w	dvtw1	Second coefficient of narrow width effect on Vth for small channel length	5.3e6	1/m	
Dvt2w	dvt2w	Body-bias coefficient of narrow width effect for small channel length	-0.032	1/V	
μ0	u0	Mobility at Temp = Tnom NMOSFET PMOSFET	 670.0 250.0	$cm^2/V/sec$	

DC Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Ua	ua	First-order mobility degradation coefficient	2.25E-9	m/V	
Ub	ub	Second-order mobility degradation coefficient	5.87E-19	$(m/V)^2$	
Uc	uc	Body-effect of mobility degradation coefficient	mobmod =1, 2: -4.65e-11 mobmod =3: -0.046	m/V^2 1/V	
vsat	vsat	Saturation velocity at Temp = Tnom	8.0E4	m/sec	
A0	a0	Bulk charge effect coefficient for channel length	1.0	none	
Ags	ags	gate bias coefficient of Abulk	0.0	1/V	
B0	b0	Bulk charge effect coefficient for channel width	0.0	m	
B1	b1	Bulk charge effect width offset	0.0	m	
Keta	keta	Body-bias coefficient of bulk charge effect	-0.047	1/V	
A1	a1	First non-saturation effect parameter	0.0	1/V	
A2	a2	Second non-saturation factor	1.0	none	
Rdsw	rdsw	Parasitic resistance per unit width	0.0	Ω-μm^{Wr}	
Prwb	prwb	Body effect coefficient of Rdsw	0	$V^{-1/2}$	
Prwg	prwg	Gate bias effect coefficient of Rdsw	0	1/V	

DC Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Pdiblc1	pdiblc1	First output resistance DIBL effect correction parameter	0.39	none	
Pdiblc2	pdiblc2	Second output resistance DIBL effect correction parameter	0.0086	none	
Pdiblcb	pdiblcb	Body effect coefficient of DIBL correction parameters	0	1/V	
Drout	drout	L dependence coefficient of the DIBL correction parameter in Rout	0.56	none	
Pscbe1	pscbe1	First substrate current body-effect parameter	4.24E8	V/m	
Pscbe2	pscbe2	Second substrate current body-effect parameter	1.0E-5	m/V	
Pvag	pvag	Gate dependence of Early voltage	0.0	none	
δ	delta	Effective Vds parameter	0.01	V	
Ngate	ngate	poly gate doping concentration	0	cm^{-3}	
$\alpha 0$	alpha0	The first parameter of impact ionization current	0	m/V	
$\beta 0$	beta0	The second parameter of impact ionization current	30	V	
Rsh	rsh	Source drain sheet resistance in ohm per square	0.0	Ω/ square	
Js0sw	jssw	Side wall saturation current density	0	A/m	
Jso	js	Source drain junction saturation current per unit area	1.E-4	A m^2	

AC and Capacitance Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Pbsw	pbsw	Source/drain side junction built-in potential	1.0	V	
Pb	pb	Bottom built-in potential	1.0	V	
Pbswg	pbswg	Source/Drain gate sidewall junction built-in potential	Pbsw	V	
CGS1	cgs1	Light doped source-gate region overlap capacitance	0.0	F/m	
CGD1	cgd1	Light doped drain-gate region overlap capacitance	0.0	F/m	
CKAPPA	ckappa	Coefficient for lightly doped region overlap capacitance Fringing field capacitance	0.6	F/m	
Cf	cf	fringing field capacitance	calculated	F/m	nC-3
CLC	clc	Constant term for the short channel model	0.1E-6	m	
CLE	cle	Exponential term for the short channel model	0.6	none	
DLC	dlc	Length offset fitting parame-ter from C-V	lint	m	
DWC	dwc	Width offset fitting parameter from C-V	wint	m	
Vfb	vfb	Flat-band voltage parameter (for capmod=0 only)	-1	V	

A.4 NQS Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Elm	elm	Elmore constant of the channel	5	none	

A.5 dW and dL Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Wl	wl	Coefficient of length dependence for width offset	0.0	m^{Wln}	
Wln	wln	Power of length dependence of width offset	1.0	none	
Ww	ww	Coefficient of width dependence for width offset	0.0	m^{Wwn}	
Wwn	wwn	Power of width dependence of width offset	1.0	none	
Wwl	wwl	Coefficient of length and width cross term for width offset	0.0	$m^{Wwn+Wln}$	
Ll	ll	Coefficient of length dependence for length offset	0.0	m^{Lln}	
Lln	lln	Power of length dependence for length offset	1.0	none	

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Lw	lw	Coefficient of width dependence for length offset	0.0	$_{m}^{Lwn}$	
Lwn	lwn	Power of width dependence for length offset	1.0	none	
Lwl	lwl	Coefficient of length and width cross term for length offset	0.0	$_{m}^{Lwn+Ln}$	

A.6 Temperature Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Tnom	tnom	Temperature at which parameters are extracted	27	°C	
µte	ute	Mobility temperature exponent	-1.5	none	
Kt1	kt1	Temperature coefficient for threshold voltage	-0.11	V	
Kt1l	kt1l	Channel length dependence of the temperature coefficient for threshold voltage	0.0	V*m	
Kt2	kt2	Body-bias coefficient of Vth temperature effect	0.022	none	

Temperature Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Ua1	ua1	Temperature coefficient for Ua	4.31E-9	m/V	
Ub1	ub1	Temperature coefficient for Ub	-7.61E-18	$(m/V)^2$	
Uc1	uc1	Temperature coefficient for Uc	mob-mod=1, 2: -5.6E-11 mob-mod=3: -0.056	m/V^2 1/V	
At	at	Temperature coefficient for saturation velocity	3.3E4	m/sec	
Prt	prt	Temperature coefficient for Rdsw	0	Ω-μm	
At	at	Temperature coefficient for saturation velocity	3.3E4	m/sec	
nj	nj	Emission coefficient of junction	1	none	
XTI	xti	Junction current temperature exponent coefficient	3.0	none	

A.7 Flicker Noise Model Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Noia	noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18	none	
Noib	noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3	none	
Noic	noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12	none	
Em	em	Saturation field	4.1e7	V/m	
Af	af	Frequency exponent	1	none	
Ef	ef	Flicker exponent	1	none	
Kf	kf	Flicker noise parameter	0	none	

A.8 Process Parameters

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit	Note
Tox	tox	Gate oxide thickness	1.5e-8	m	
Xj	xj	Junction Depth	1.5e-7	m	
$\gamma 1$	gamma1	Body-effect coefficient near the surface	calculated	$V^{1/2}$	nl-4